Product How-to: Ultra-low noise linear regulators for powering PLL/VCO and clocking ICs

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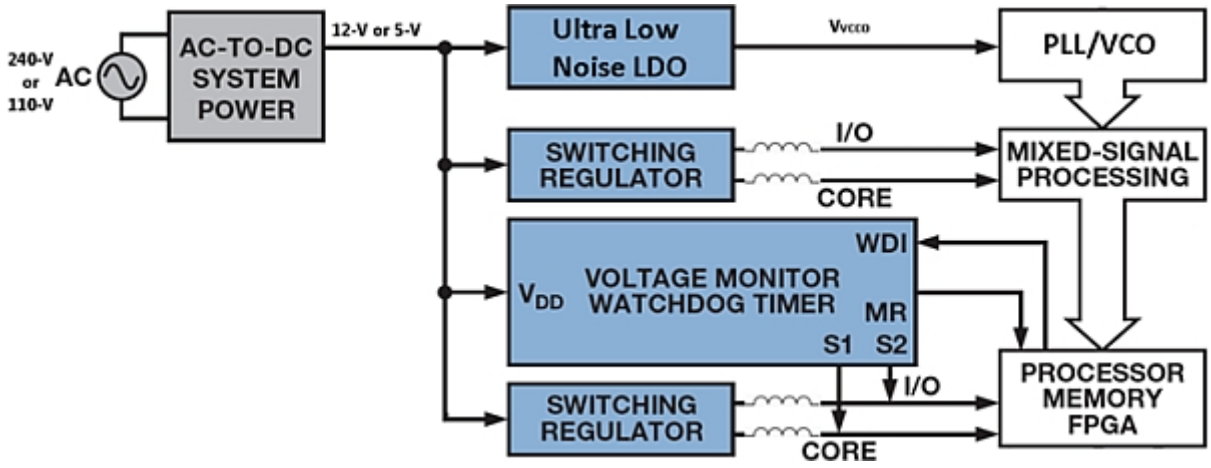
Wideband communication systems usually require an ultra-low noise regulator to power the VCOs and PLLs. The regulator must also be able to reject any ripple presented at its input. In a typical system, an ac input is converted to an isolated dc supply rail, –48-V, for example. This rail is then converted to an isolated 12-V or 5-V system rail that powers the main components in the communication system.

This 12-V or 5-V system rail is generated by inductive switching elements that create ripple and noise on the rail. To provide a clean power rail, an ultralow-noise regulator is required to generate the 5-V, 3.3-V or 2.5-V rail used to power the wideband PLL and VCO. Any noise or ripple present on the 5-V, 3.3-V or 2.5-V rail will degrade the performance of the PLL or VCO.



Ultralow-Noise LDOs – ADM7150 & ADM7151

The fixed-output ADM7150 and adjustable-output ADM7151 ultralow-noise linear regulators for RF signal devices operate from 4.5 V to 16 V, provide up to 800 mA of output current, and support output voltages from an input voltage of 1.5 to 5.0 V. The LDOs achieve 1.4-nV/√Hz output noise spectral density (NSD) from 10 kHz to 1 MHz, significantly reducing VCO phase noise in point-t-

-point microwave radios, satellite communications, defense electronics, and other wideband systems. In addition, a user-adjustable capacitor can significantly reduce low-frequency noise (8 nV/√Hz at 100 Hz) for precision analog front-end measurement systems. The total solution size is only 7.62 mm × 5.21 mm.

Noise Spectral Density and Power Supply Rejection (PSRR)

The ADM7150 & ADM7151 typical output noise is 1.0 µV rms from 100 Hz to 100 kHz for fixed-output-voltage options, with 1.7 nV/√Hz noise spectral density from 10 kHz to 1 MHz. Using an advanced proprietary architecture, the regulators provide high power supply rejection (>90 dB from 1 kHz to 1 MHz), and achieve excellent line and load transient response with a 10 µF ceramic output capacitor.

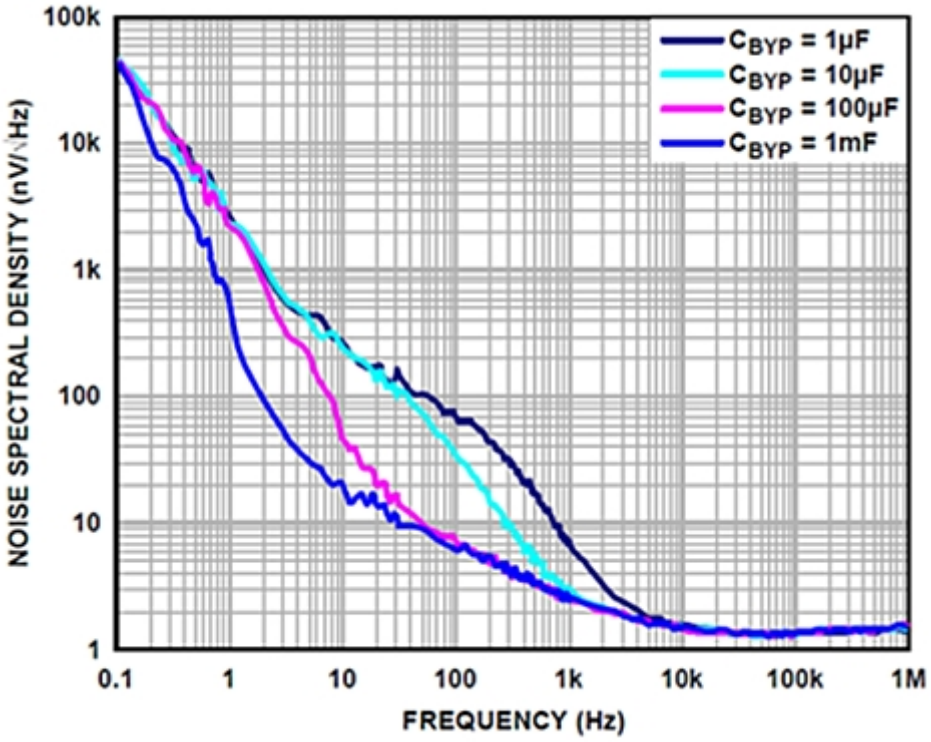


Figure 3: Noise Spectral Density (NSD) vs. Frequency for various V_{BYP}

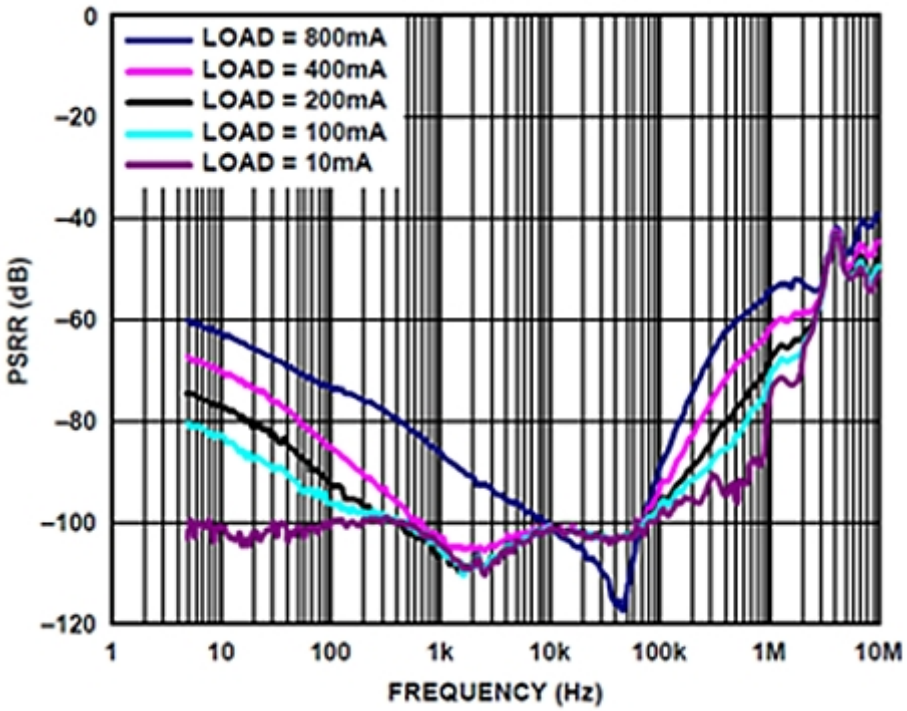


Figure 4: Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 5V, V_{IN} = 6.2V

ADM7150 Design Examples

This example shows the ADF5355, Microwave Wideband Synthesizer with Integrated VCO when powered by the ADM7150 Ultra Low Noise LDO.

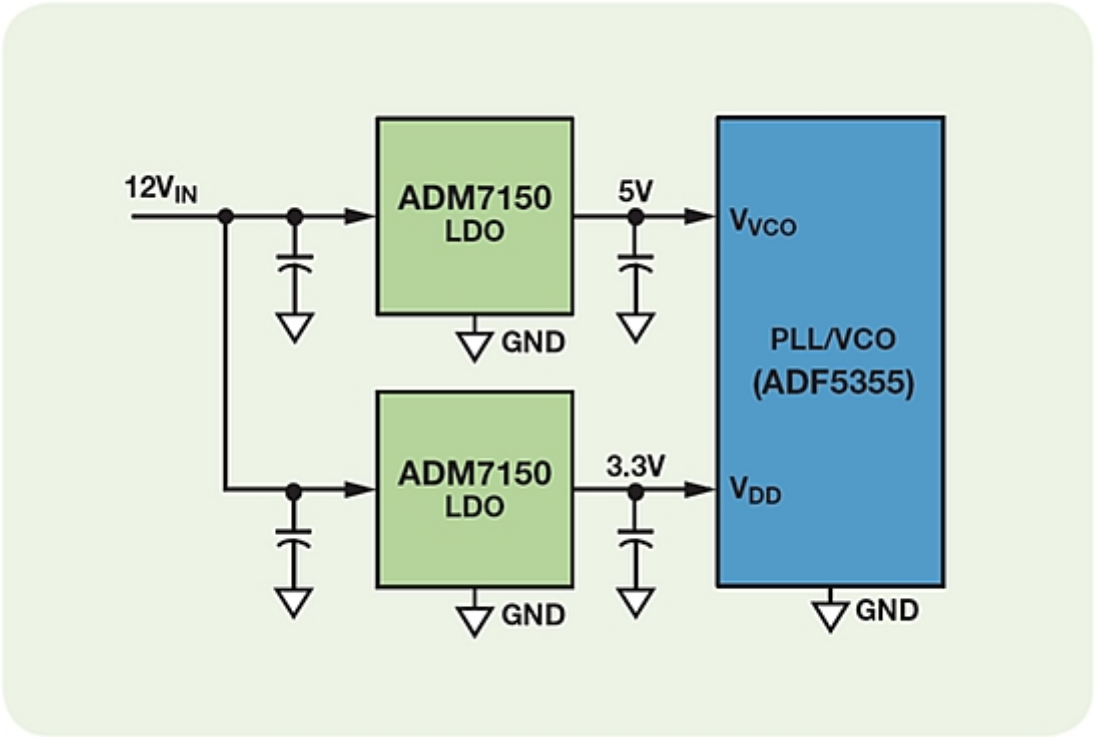


Figure 5: PLL/VCO apps diagram

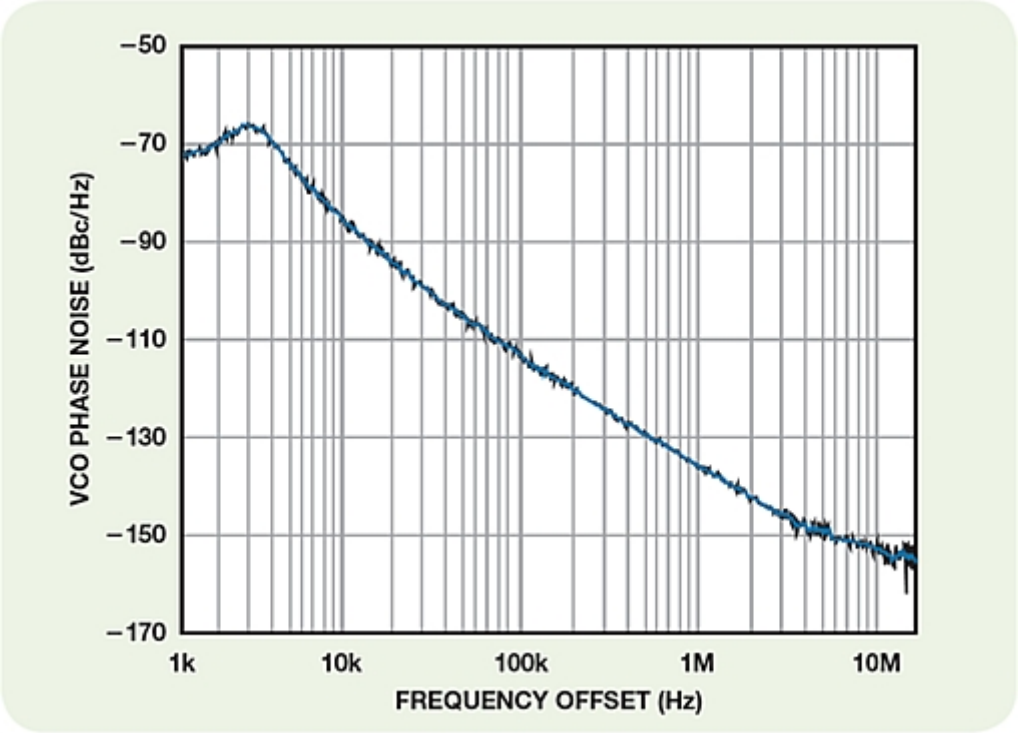
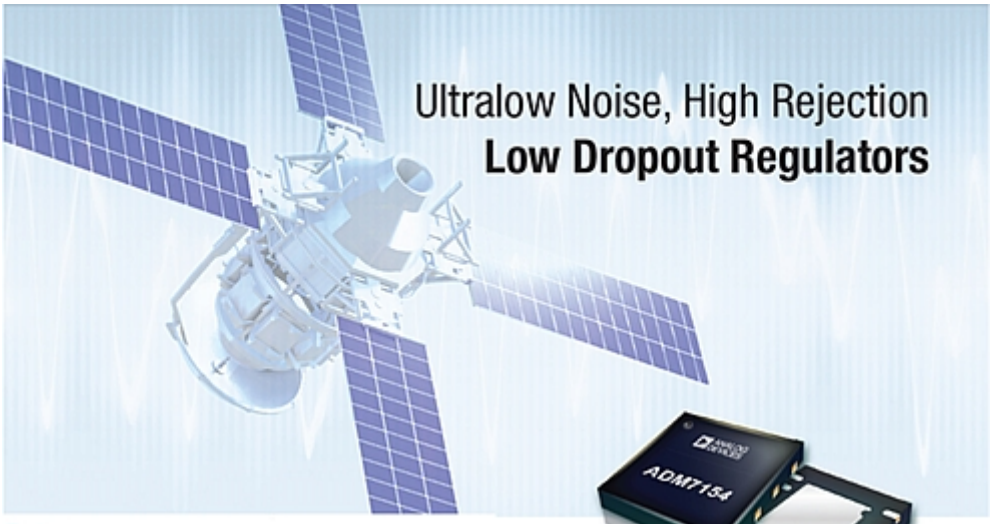


Figure 6: ADF5355 VCO noise, powered by ADM7150

Ultralow-Noise LDOs – ADM7154 & ADM7155

Ultralow-Noise LDOs – ADM7154 & ADM7155

The fixed-output ADM7150 and adjustable-output ADM7151 are ultralow noise LDO (low dropout) regulators for RF (radio frequency) signal devices. The ADM7154 & ADM7155 operate from 2.3 V to 5.5 V input voltage range, provide up to 600 mA of output current, and support output voltages from 1.2 V to 3.3 V. The LDOs achieve an output NSD (noise spectral density) of 1.5 nV/√Hz above 100 kHz, which significantly reduces VCO (voltage controlled oscillator) phase noise in point to point microwave radios, satellite communications, defense electronics, and other wideband applications.



Features

- V_{IN} range: 2.3 V to 5.5 V
- Fixed/adjustable output voltage range: 1.2 V to 3.3 V
- I_{OUT} max: 600 mA
- Low noise (C_{BYP} = 1 µF)
  - 0.9 µV rms total integrated noise from 100 Hz to 100 kHz
  - 2 nV/√Hz above 4 kHz
- Power supply rejection ratio (PSRR):
  - 90 dB from 1 kHz to 100 kHz
    - V_{IN} = 3.8 V, V_{OUT} = 3.3 V @ 600 mA
  - 58 dB at 1 MHz
    - V_{IN} = 3.8 V, V_{OUT} = 3.3 V @ 600 mA
- 8-lead LFCSP and 8-lead SOIC packages

Applications

- Regulated power noise sensitive applications
- RF mixers, phase-locked loops (PLLs)
- Voltage controlled oscillators (VCOs)
- PLLs with integrated VCOs
- Communications and infrastructure
- Cable digital-to-analog converter (DAC) drivers
- Backhaul and microwave links

Noise Spectral Density and Power Supply Rejection (PSRR)

The ADM7154 & ADM7155 typical output noise is 0.9 µV rms from 100 Hz to 100 kHz for fixed-output-voltage options, with 1.5 nV/√Hz noise spectral density from 10 kHz to 1 MHz. Using an advanced proprietary architecture, the regulators provide high power supply rejection (PSRR of 90 dB from 200 Hz to 200 kHz; 58 dB at 1 MHz), and achieve excellent line and load transient response with a 10 µF ceramic output capacitor.

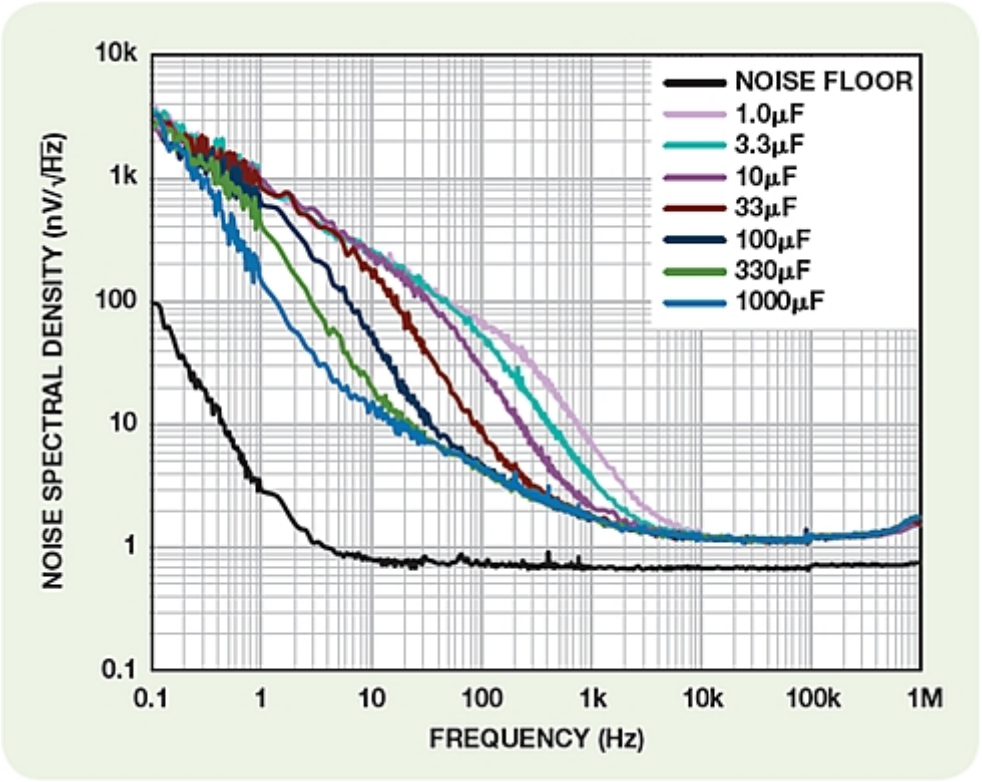


Figure 8: ADM7154 noise spectral density

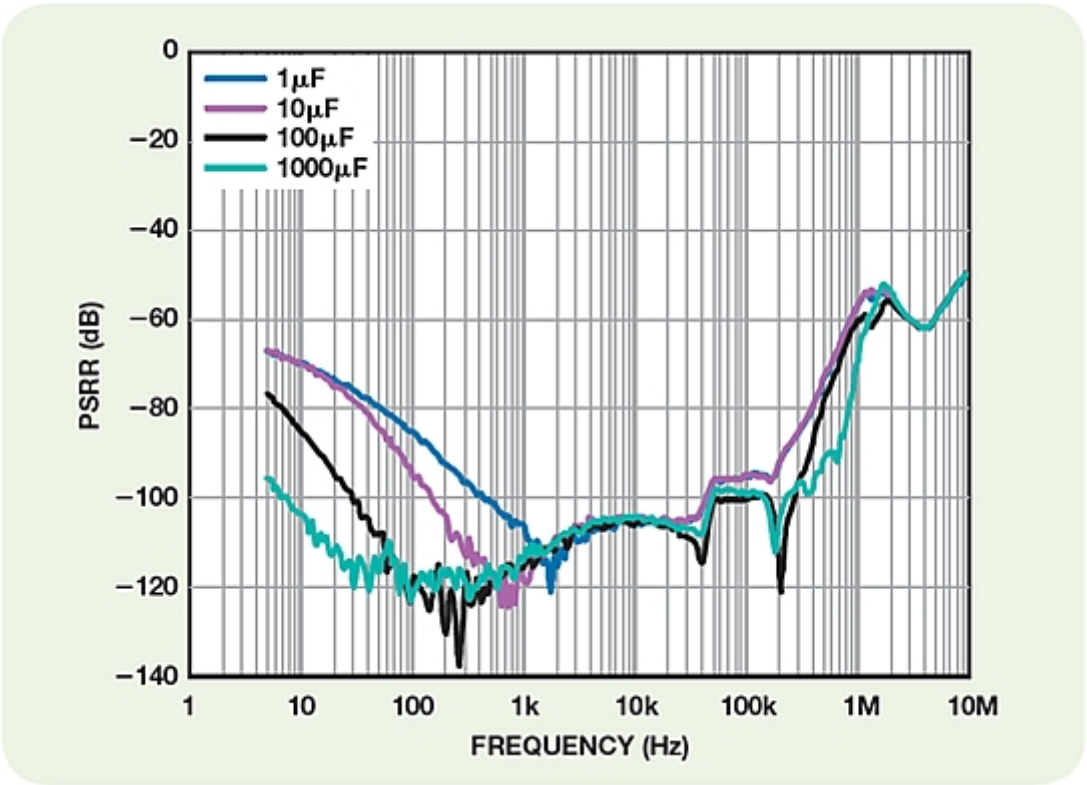


Figure 9: ADM7154 PSRR vs. Frequency, V_{OUT} = 3.3V, 400 mA load, 500 mV headroom

ADM7154 Design Examples

This example shows the ADM7150 powering a VCO (Voltage Controller Oscillator) and the ADM7154 powering the AD9525, Low Jitter Clock Generator with Eight LVPECL Outputs.

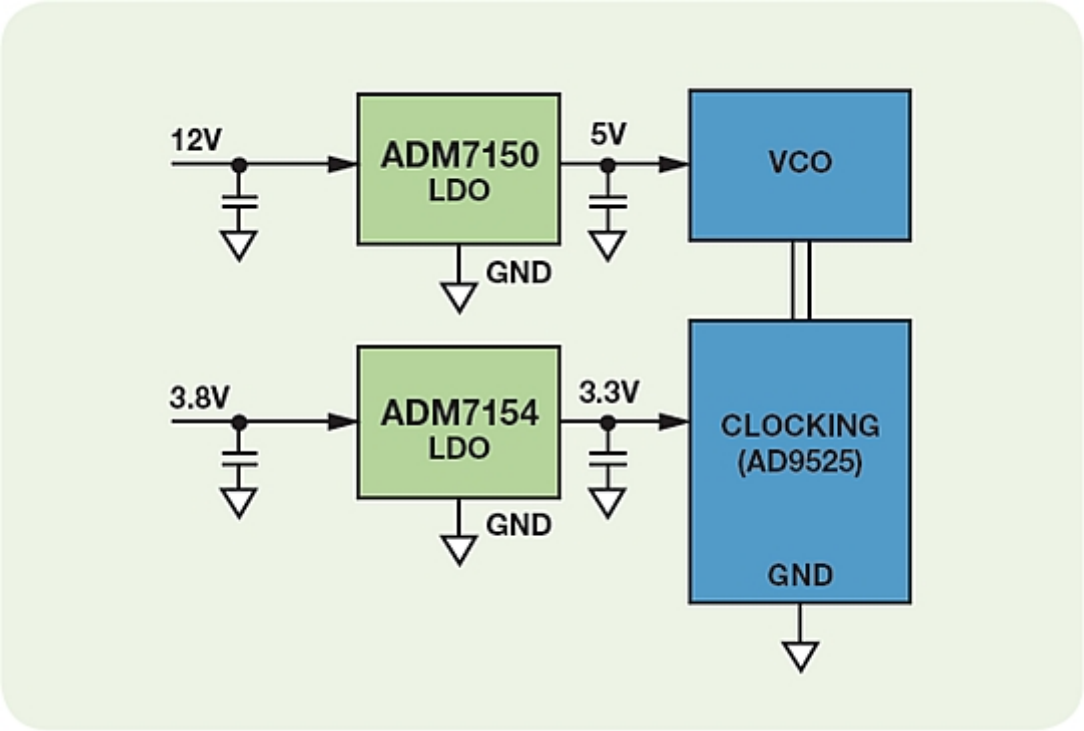


Figure 10: Clocking apps diagram

Online Tools and Resources for Ultra Low Noise LDOs - ADIsimPower

Analog Devices ADIsimPower collection of design tools, produce complete power designs using real component behavior and is optimized for your design goals (efficiency, cost, size or component count). Each tool generates a schematic, bill of materials, and performance data such as bode plot, transient response, efficiency, or thermal stresses on components.

Conclusion

The emergence of wideband communications is driving the need for newer ultralow noise LDOs for powering the next generation of PLL/VCO and clocking devices. The ADM7150, ADM7151, ADM7154 and ADM7155 LDOs reduce noise spectral density by a factor of two and provide the lowest phase noise for powering VCOs and the lowest jitter performance for powering clocks in microwave systems.