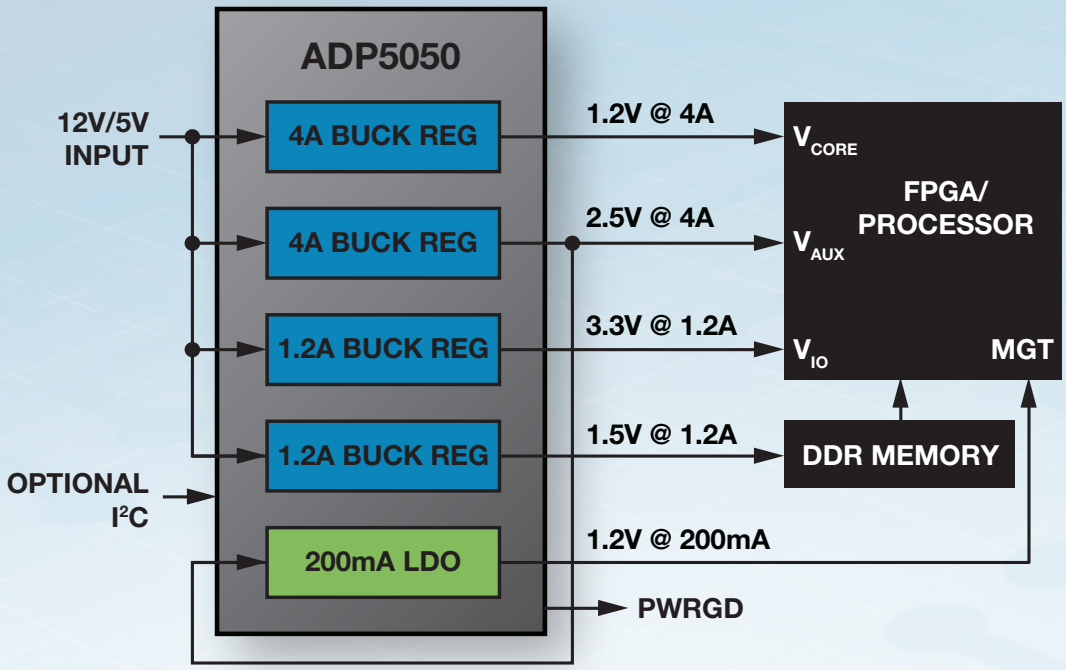
Integrated Power Management Solutions

ADI Announces a New Family of Multichannel Regulators

Ultrasmall 12 V/5 V Quad Buck + LDO in LFCSP



- *Fixed and Adjustable Output Voltages*
- *Wide Range of Switching Frequency Operation (250 kHz to 1.4 MHz)*
- *Resistor Programmable Current Limit on Buck 1 and Buck 2 (4 A, 2.5 A, 1.2 A)*
- *Simple Power Supply Sequencing*
- *Frequency Synchronization Input or Output*
- *LDO or POR/WDI Options*

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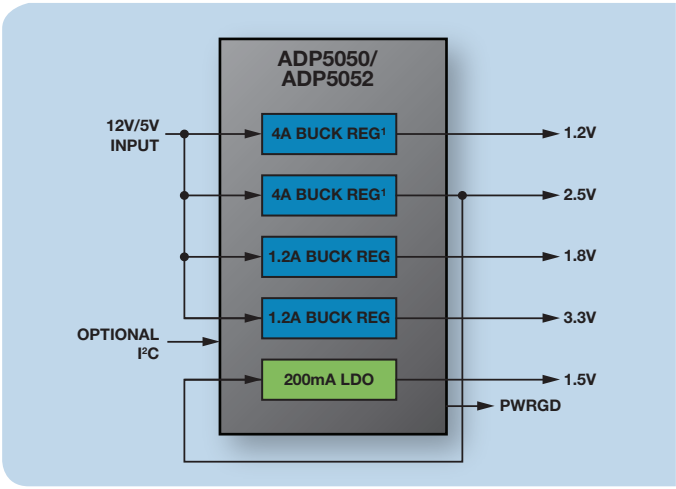
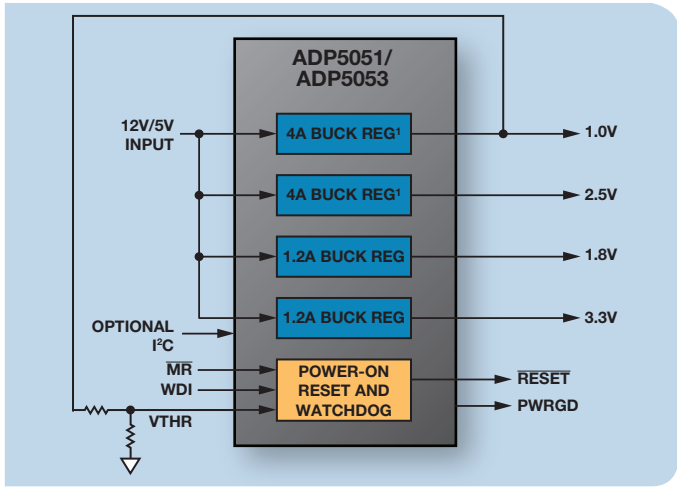
ANALOG DEVICES

Quad Buck Switching Regulator with LDO or POR/WDI in LFCSP



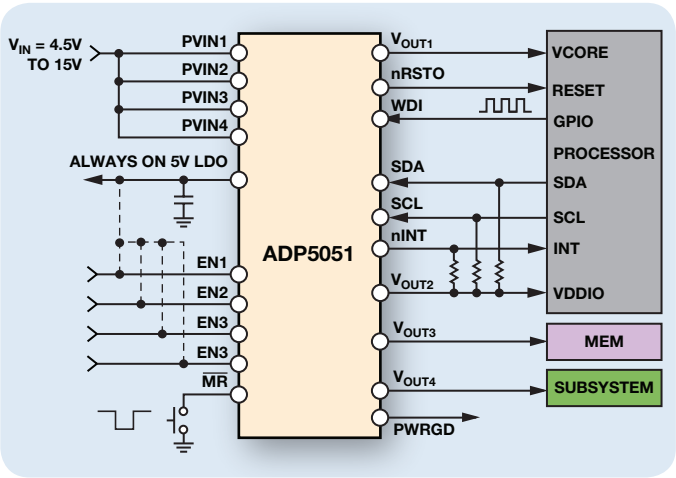


[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

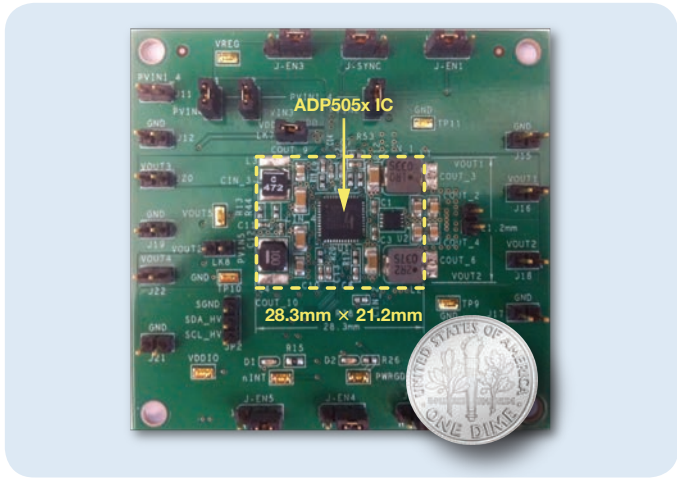
Key Features

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 KHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory
- Pseudo-DVS: dynamic voltage scaling
- I²C interface with interrupt supportive on fault condition
- CH1/CH2: programmable 1.2 A/2.5 A/4 A sync buck regulator with low-side FET driver
- CH3/CH4: 1.2 A sync buck regulator
- CH5: 200 mA low-dropout LDO or watchdog timer and power on reset
- Precision enable on 0.8 V accurate threshold
- Active output discharge switch
- FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag on selective channels
- Startup with the precharged output
- 48-lead, 7 mm × 7 mm LFCSP package
- −40°C to +125°C junction temperature
- I²C functionality

I²C Functionality



ADP5051 application diagram featuring the I²C interface.



ADP505x solution size only 28.3 mm × 21.2 mm.

Option 1: Resistor programmable output voltage from 0.8 V to V_{IN} × 0.85

Option 2: Fixed output voltage with I²C programmability with these ranges for each channel

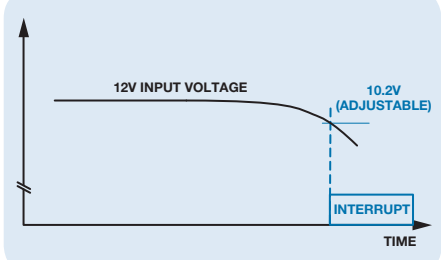
[CH1: 0.85V~1.60V, 25mV STEP]

[CH2: 3.3V~5.0V, ~300mV STEP]

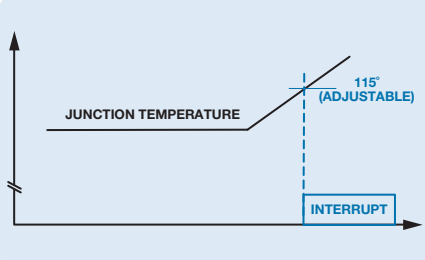
[CH3: 1.2V~1.80V, 100mV STEP]

[CH4: 2.5V~5.5V, 100mV STEP]

ADP505x output voltage options.



Low input voltage detection on PVIN1.

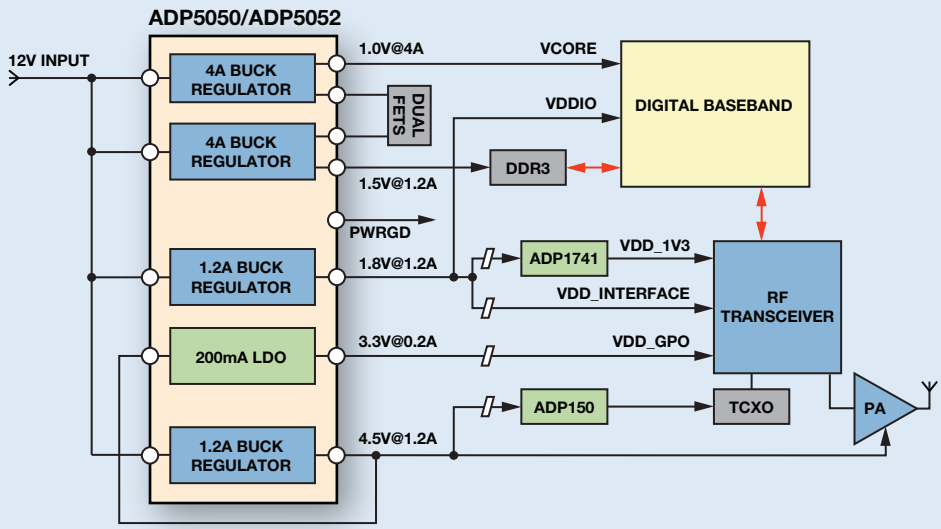


Overheat function on junction temperature.

Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I^2C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							

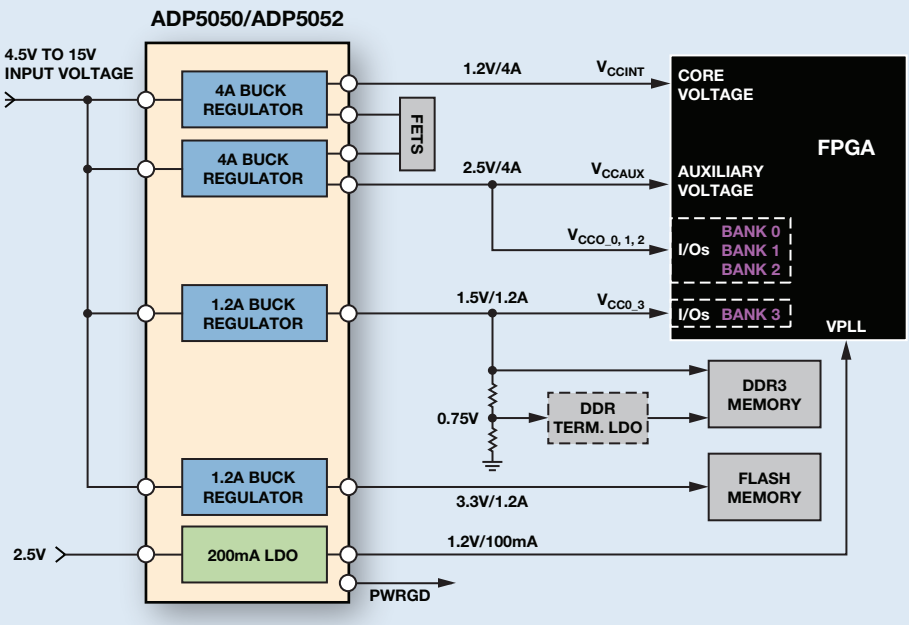
[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

ADP5050/ADP5052 Small Cell Applications Example



Support flexible power-up sequence by precision enable and PWRGD.

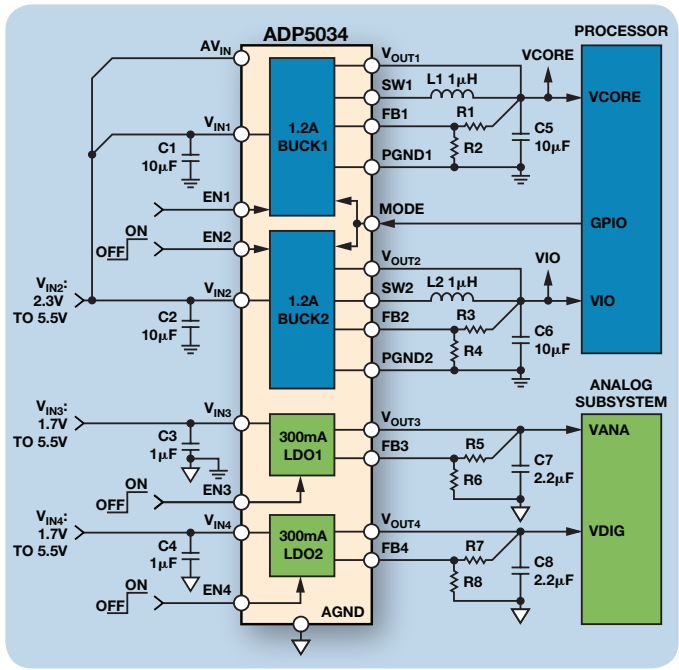
ADP5050/ADP5052 Power for FPGA Applications Example



Dual, 3 MHz, 1.2 A Buck Regulator with Two 300 mA LDOs in LFCSP

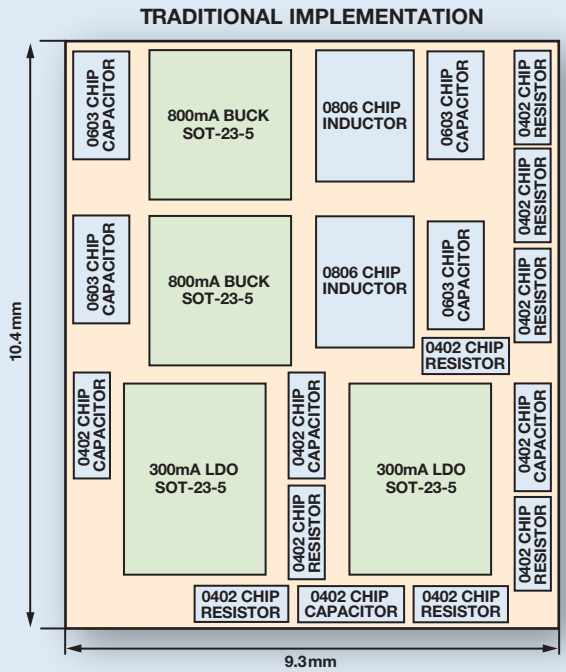
Key Features

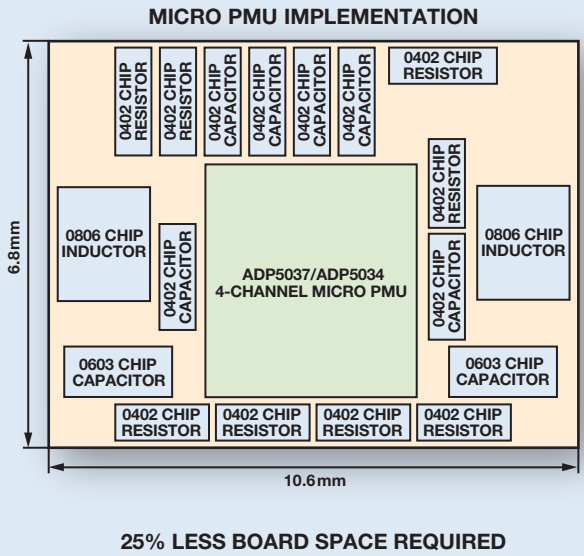
- Input voltage range: 2.3 V to 5.5 V
- Two 1.2 A buck regulators
- Two 300 mA LDOs
- Regulator accuracy: ±1.8%
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Factory-programmable or external adjustable V_{OUTx}
- Buck 1 and Buck 2 key specifications
  - High efficiency: up to 96%
  - Current-mode architecture
  - 3 MHz operating frequency
  - Forced PWM and auto PWM/PSM modes
  - Out of phase operation for reduced input filtering
- LDO1 and LDO2 key specifications
  - Stable with 1 µF ceramic output capacitors
  - High PSRR: 65 dB PSRR 1 kHz to 10 kHz
  - Low output noise: 80 µV rms typical output noise at V_{OUT3} = 2.5 V
  - Low dropout voltage: 150 mV @ 300 mA load
  - Low input supply voltage from 1.7 V to 5.5 V
- −40°C to +125°C junction temperature
- ADP5034: 24-lead, 4 mm × 4 mm LFCSP package
- ADP5034: 28-lead TSSOP
- ADP5033: 16-lead WLCSP



ADP5034 functional block diagram.

ADP5034 Micro PMU Advantages

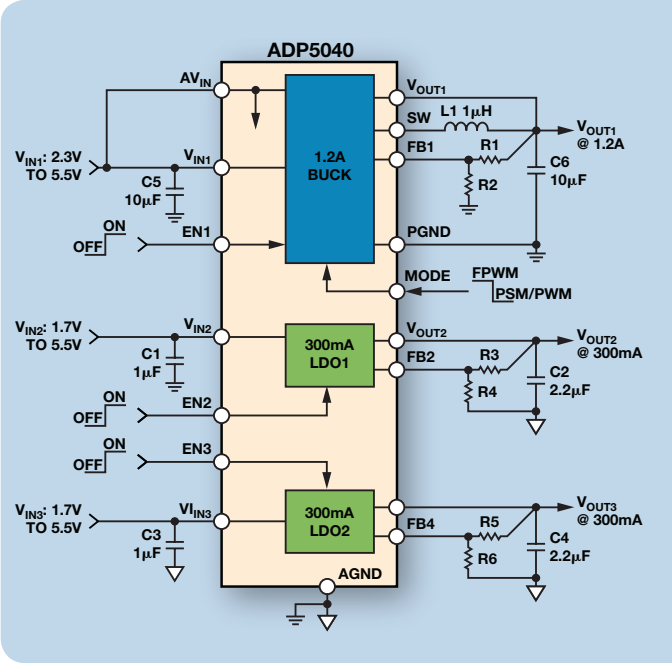




25% LESS BOARD SPACE REQUIRED

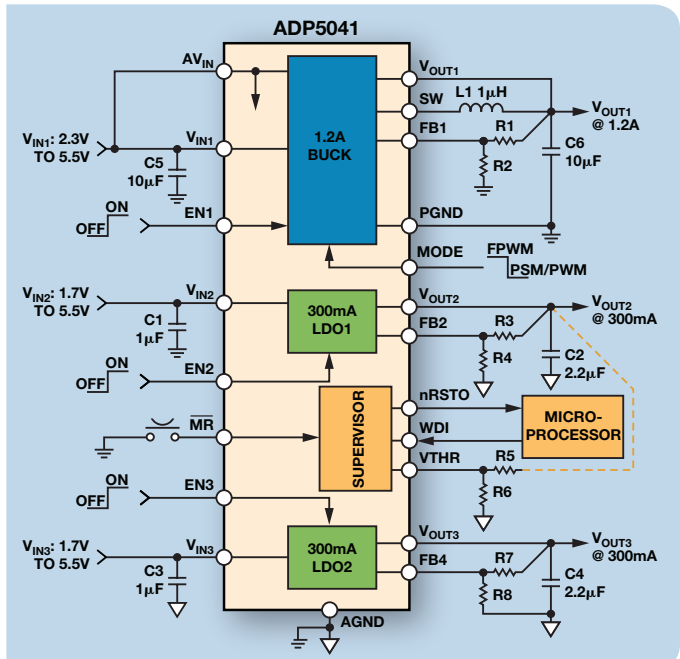
- Lower cost, requires fewer external components
- Smaller board size
- Easier layout implementation
- Bucks are internally synchronized and out of phase
- Better thermal dissipation using the exposed pad

ADP5040: 1.2 A Buck and Dual 300 mA LDO with Individual Enables in LFCSP



ADP5040 functional block diagram.

ADP5041: 1.2 A Buck and Dual 300 mA LDO, Supervisory, Watchdog, and Manual Reset in LFCSP

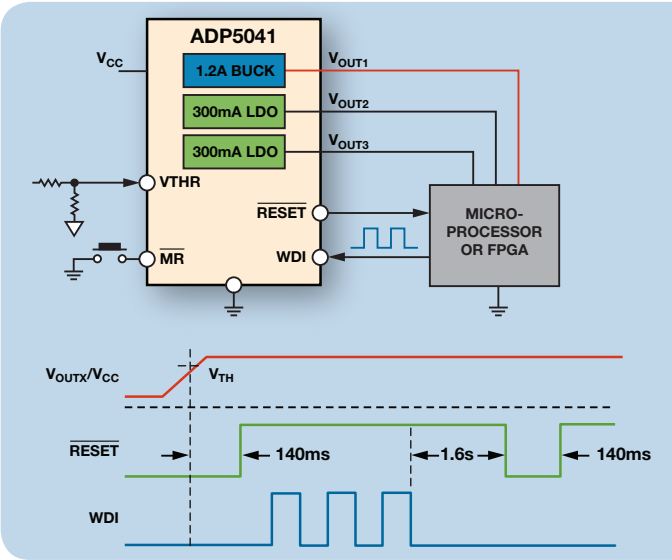


ADP5041 functional block diagram.

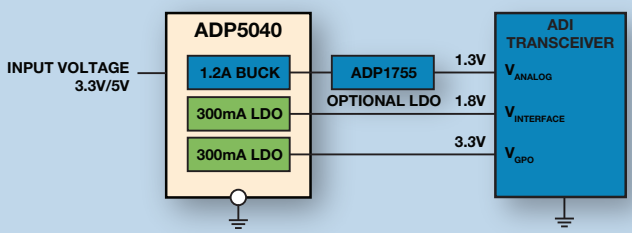
Key Features

- Input voltage range: 2.3 V to 5.5 V
- One 1.2 A buck regulator, fixed and adjustable output voltages, up to 96% efficiency
- Two 300 mA LDOs, fixed and adjustable outputs
- 20-lead, 4 mm × 4 mm LFCSP package
- Initial regulator accuracy: ±1%
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Open-drain processor reset with external adjustable threshold monitoring
- ±1.5% threshold accuracy over the full temperature range
- Guaranteed reset output valid to V_{CC} = 1 V
- Manual reset input
- Watchdog refresh input
- Two reset timeout options: 20 ms and 140 ms (minimum)
- Two watchdog timeout options: 102 ms and 1600 ms (typical)

ADP5041 Delivers Improved System Reliability by Integrating Power-On Reset and Watchdog Functionality



±1.5% trip threshold accuracy to monitor low voltage core rails.



- Single-chip power companion IC for wideband RF transceivers.
- Small power management footprint, 3 MHz buck regulator uses very small multilayer inductor.

Powering noise sensitive RF transceiver.

Integrated Power Management Solutions (Micro PMUs)

Part Number	Product Description	V_{IN} (V)	V_{OUT} (V)	Number of Outputs	Output Current (mA)	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Key Features	Package	Price ($U.S.)
ADP5022	Dual, 3 MHz buck with 150 mA LDO	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8	2 × buck	600	—	—	—	—	Mode pin, individual enable pins	16-ball WLCSP	1.80
		LDO: 1.7 to 5.5	LDOs: 3.3, 3.0, 2.9, 2.8, 2.775, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	1 × LDO	150							
ADP5023	Dual, 800 mA buck with 300 mA LDO	Bucks: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.59
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	1 × LDO	300							
ADP5024	Dual, 1.2 A buck with 300 mA LDO	Bucks: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.79
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	1 × LDO	300							
ADP5033	Dual, 3 MHz buck regulator with dual LDO	Bucks: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Mode pin, two enable pins	16-ball WLCSP	1.90
		LDOs: 1.7 to 5.5	LDOs: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	2 × LDO	300							
ADP5034	Dual, 3 MHz buck regulator with dual LDO	Bucks: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP 28-lead TSSOP	1.99
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	2 × LDO	300							
ADP5037	Dual, 3 MHz, 800 mA buck regulator with dual 300 mA LDO	Bucks: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.69
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	2 × LDO	300							
ADP5040	3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	—	—	—	Individual enable pins, mode pin	20-lead LFCSP	1.39
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	2 × LDO	300							
ADP5041	3 MHz buck regulator with dual LDO, supervisor, and watchdog timer	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	0.5 (adj)	20, 140	102, 1600	Individual enable pins and supervisor, WDI, mode pin and MR pin	20-lead LFCSP	1.79
		LDOs: 1.7 to 5.5	Adj (0.8 to 4.75)	2 × LDO	300							
ADP5042	3 MHz buck regulator with dual LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	1 × buck	800	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin and MR pin	20-lead LFCSP	1.99
		LDOs: 1.7 to 5.5	LDOs: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1, 0.9, 0.8	2 × LDO	300	—						
ADP5043	3 MHz buck regulator with LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	1 × buck	800	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin and MR pin	20-lead LFCSP	1.79
		LDO: 1.7 to 5.5	LDOs: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1, 0.9, 0.8	1 × LDO	300							
ADP320	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3; LDO2: 1.8, 3.3; LDO3: 1.5	3 × LDO	200	—	—	—	—	Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP322	Triple, 200 mA LDO	1.8 to 5.5	LDO1: 3.3, 2.8, 2.5; LDO2: 2.8, 2.5, 1.8; LDO3: 1.8. 1.5, 1.2	3 × LDO	200					Fixed V_{OUT} options	16-lead LFCSP	0.54
ADP323	Triple, 200 mA LDO	1.8 to 5.5	Adj (0.5 to 5)	3 × LDO	200	—	—	—	—	Adjustable V_{OUT} options	16-lead LFCSP	0.54
ADP5050 ***New***	Quad buck regulator + LDO with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	—	—	—	I²C interface with individual enable pins and power good	48-lead LFCSP	4.39
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5051 ***New***	Quad buck regulator + POR and WDI with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	I²C interface with individual enable pins and power good	48-lead LFCSP	4.59
				2 × buck	1200							
ADP5052 ***New***	Quad buck regulator + LDO	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	—	—	—	Individual enable pins with power good	48-lead LFCSP	3.59
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5053 ***New***	Quad buck regulator + POR and WDI	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	Individual enable pins with power good	48-lead LFCSP	3.79
				2 × buck	1200							

[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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