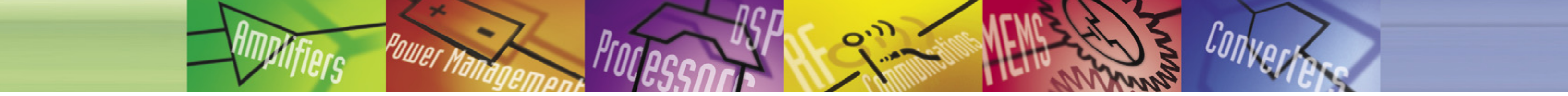
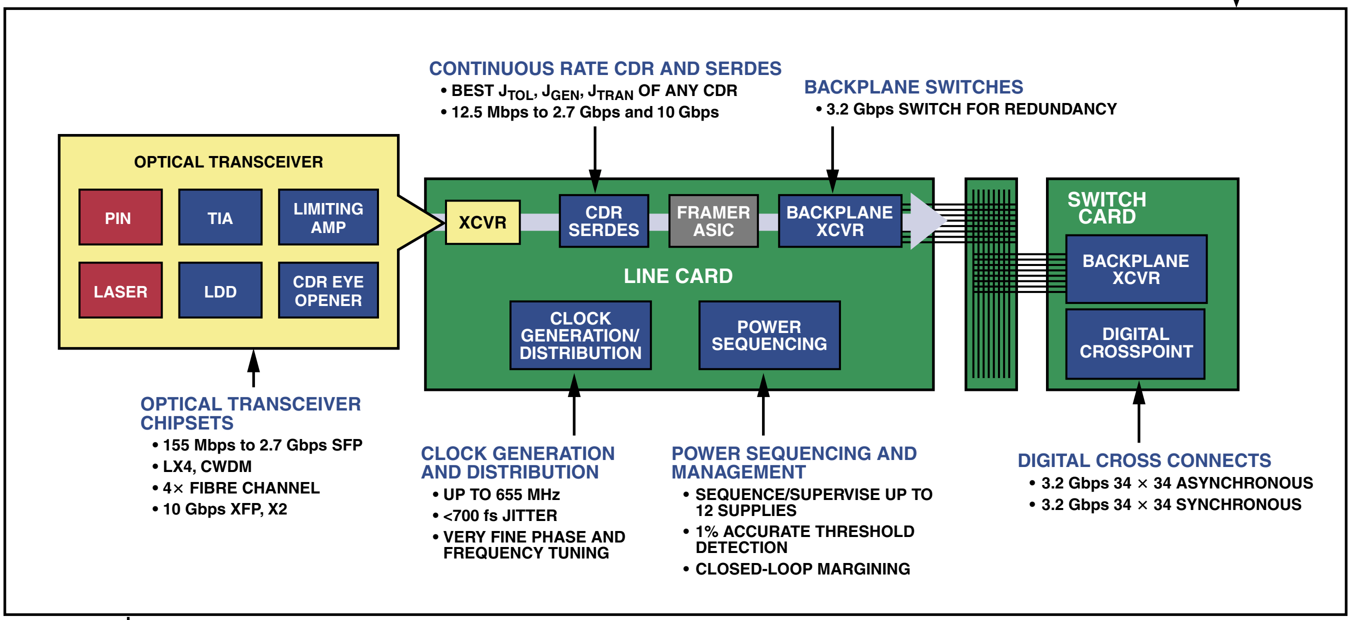


Optical and High Speed Networking



Analog Devices' optical and high speed networking ICs solve a depth and breadth of challenges faced by today's designers of datacom and telecom systems, optical modules, and subsystems. Analog Devices products address a wide range of networking applications from O/E/O conversion, clock recovery, and backplane transmission to monitoring and control of optical power, power management, and clock generation and distribution.

Inside this special product bulletin are articles, application briefs, and selection tables of ADI's high performance ICs for optical and high speed networking applications, all of which have been designed to help you solve your networking problems simply and quickly, without compromising performance.

INNOVATION • PERFORMANCE • EXCELLENCE
40 years
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ANALOG DEVICES

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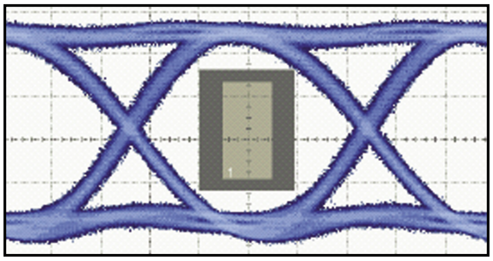
XFP Chipset and Reference Design Simplifies 10 Gbps Transceivers

Analog Devices introduces a 10 Gbps chipset that offers low power and the highest performance for receive sensitivity and transmit eye quality. Best in class jitter performance of the XFP signal conditioner increases robustness and minimizes interoperability issues. The companion reference design simplifies evaluation and speeds time to market. The reference design includes XFP boards, Gerber files, microcontroller software, and a GUI interface.

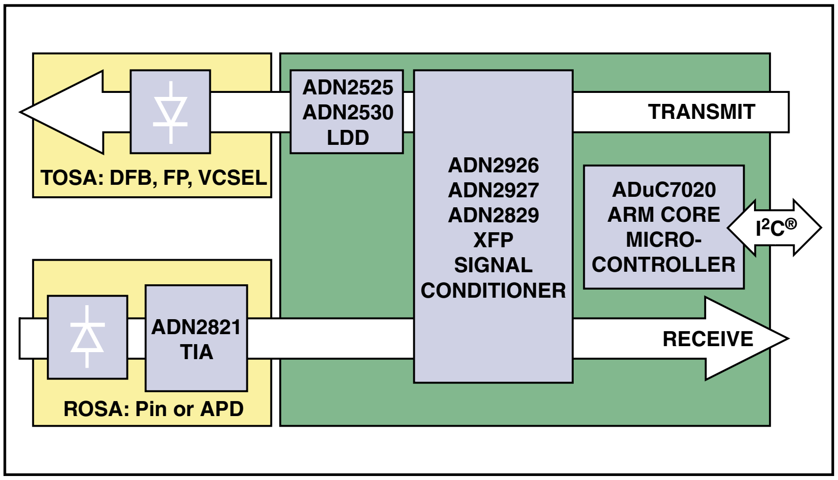
Features

- 9.9 Gbps to 11.1 Gbps data rate
- DFB, FP, or VCSEL operation
- Exceeds 20% SONET optical eye margin over temperature
- –19 dBm receive sensitivity
- Unparalleled jitter performance
- Supports full digital diagnostics
- Reference design includes Gerbers, SW, BOM, host board, and GUI interface



>20% SONET optical eye margin

XFP reference design available



ADN2821 10 Gbps TIA

APDs and pins in standard low cost TO-46 cans

- –19 dBm sensitivity
- 700 nA integrated input noise
- 8.5 Gbps BW
- 3.3 V, 150 mW
- Supports APD or pin, in low cost TO-46 can
- RSSI power meter
- 0.7 mm × 1.2 mm die size
- Samples in die or ROSA format

ADN2928 Family of XFP Signal Conditioners

Best in class for J_{GEN}, J_{TRAN}, and J_{TOL}, singles or duals

- 9.9 Gbps to 11.1 Gbps
- Exceeds XFP requirements for jitter at OC192
- Lowest jitter generation: 6 mUI rms jitter
- Highest jitter tolerance: 0.6 UI p-p @ 10 MHz
- Lowest jitter transfer: 2.0 MHz OC192
- ADN2928 transceiver in 6 mm × 6 mm BGA
- ADN2827/ADN2826 standalone transmit and receive functions in a 4 mm × 4 mm LFCSP

See Page 3 for more details.

ADN2525 Differential Active Backmatch LDD

>20% SONET optical eye margin

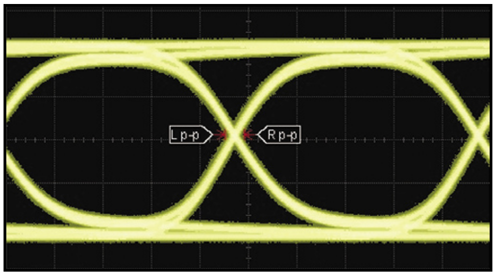
- 9.9 Gbps to 10.7 Gbps
- DFB, FP, or VCSEL operation
- Superior optical eye margins
  - SONET >20% over temperature
  - Ethernet >40% over temperature
- 750 mW typ (laser + LDD) over temperature
- Active load improves impedance matching
- 3.3 V operation, 3 mm × 3 mm LFCSP

ADN2530 Differential Active Backmatch VCSEL Driver

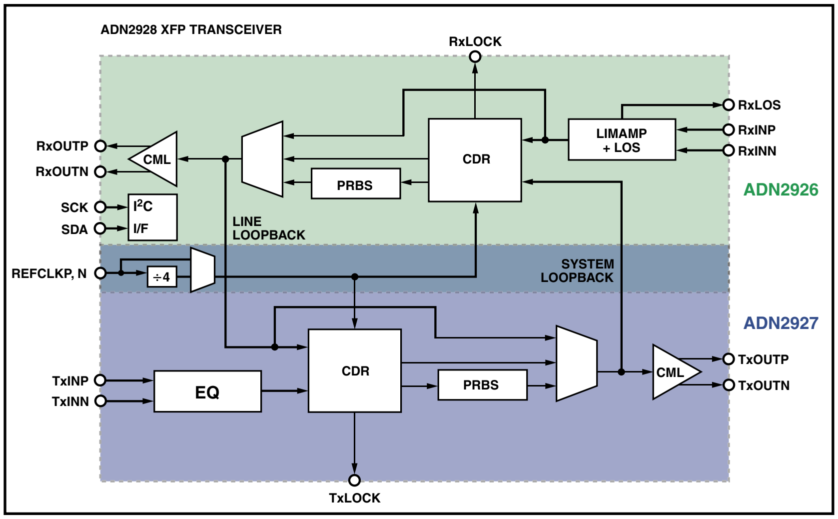
- 9.9 Gbps to 10.7 Gbps
- 300 mW typ (laser + LDD) over temperature
- SONET eye margin exceeds 20%
- Crosspoint adjust feature
- Active load improves impedance matching
- 3.3 V operation, 3 mm × 3 mm LFCSP

10 Gbps XFP Signal Conditioner

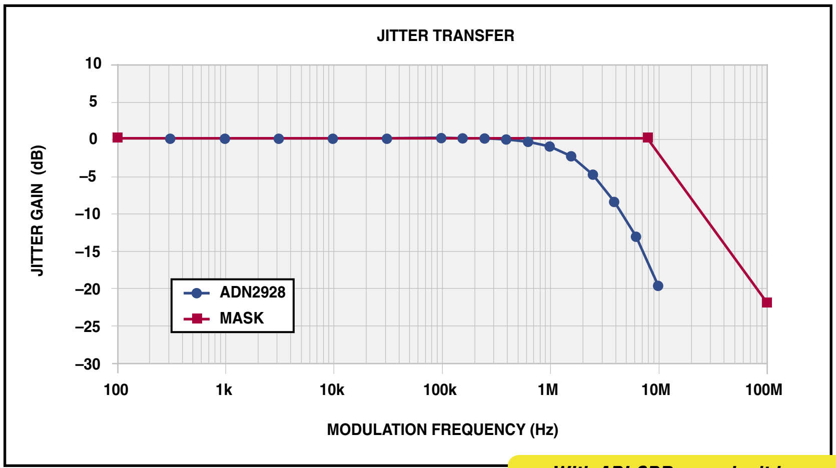
The ADN2928 family of XFP signal conditioners are the latest to employ ADI's patented performance-leading CDR architecture that maximizes both jitter tolerance and jitter transfer without compromise. The signal conditioner comes as either a bidirectional transceiver or as separate transmit and receive signal conditioner ICs, to accommodate different module layout preferences. The ADN2928 family offers unparalleled jitter performance exceeding XFP specs. Extra margin on jitter tolerance and jitter transfer specifications ensure a robust solution and solves interoperability issues.



ADN2928

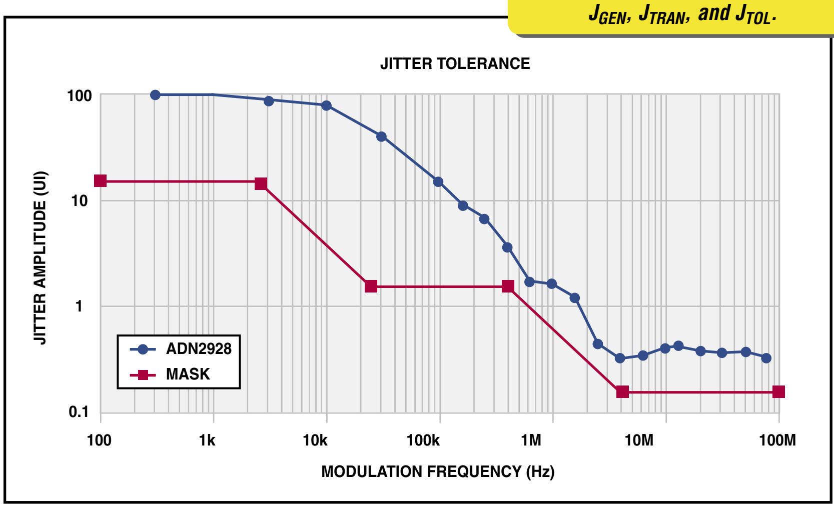


ADN2928 Functional Block Diagram



ADN2928 Jitter Transfer

With ADI CDRs you don't have to settle. You get the industry's best J_{GEN}, J_{TRAN}, and J_{TOL}.



ADN2928 Jitter Tolerance

ADN2928 XFP Transceiver

- Range: 9.9 Gbps to 11.1 Gbps
- 6 mV input sensitivity
- Lowest jitter generation: 6 mUI rms jitter @ OC192
- Highest jitter tolerance: 0.6 UI p-p @ 10 MHz OC192
- Lowest jitter transfer: 2.0 MHz OC192
- Programmable LOS indicator
- LOL indicator
- Line side and client side loopback
- 750 mW power dissipation
- 6 mm × 6 mm BGA

ADN2927 Transmit Signal Conditioner

- Equalizer with data recovery
- Range: 9.9 Gbps to 11.1 Gbps
- 375 mW power dissipation
- 4 mm × 4 mm LFCSP
- Industry-leading jitter generation

ADN2926 Receive Signal Conditioner

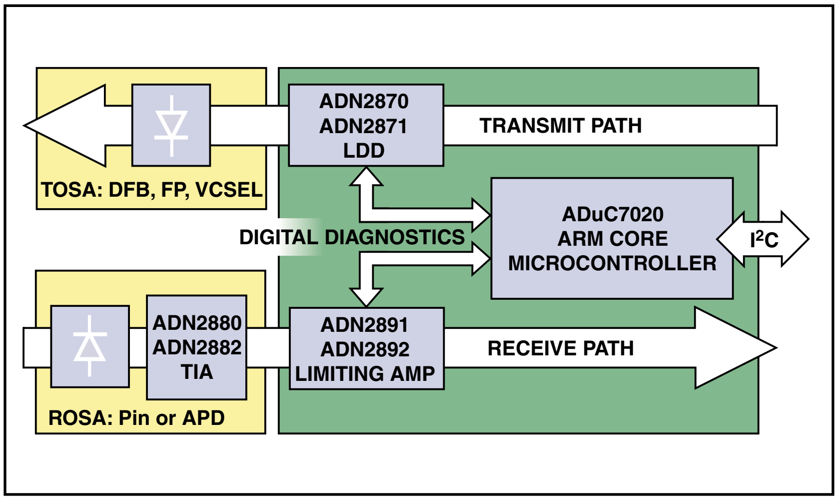
- 3 mV input sensitivity limiting amp
- Range: 9.9 Gbps to 11.1 Gbps
- 375 mW power dissipation
- 4 mm × 4 mm LFCSP
- Industry-leading jitter tolerance and transfer

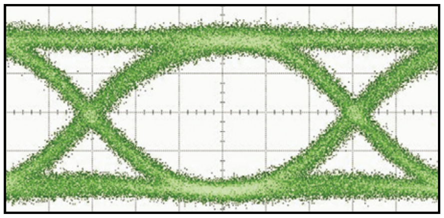
4× Fibre Channel Chipset and Reference Design

Analog Devices introduces a 4× Fibre Channel chipset that offers very low power and very high performance for receive sensitivity and transmit eye quality. Pin-compatible LDDs serve either VCSEL or DFB/FP designs. The 4× chipset is also pin- and PC board-compatible with ADI's SFP chipset. The companion reference design simplifies evaluation and speeds time to market.

Features

- Supports 1×, 2×, 4×, and 1 GE rates
- DFB, FP, or VCSEL operation
- VCSEL optical eye margin exceeds 40%
- –18 dBm receive sensitivity (850 nm pin)
- Supports full SFF-8472 digital diagnostics
- Reference design includes Gerbers, SW, BOM, host board, and GUI interface
- Best in class performance for power, sensitivity, and eye quality
- All parts pin-compatible with SONET SFP design





Optical eye margin exceeds 40% with 4 Gbps VCSEL

ADN2882 4 Gbps TIA with –18 dBm Sensitivity

- 400 nA integrated input noise
- 3.2 Gbps BW
- 5 kΩ transimpedance
- 3.3 V, 100 mW
- Optional RSSI power meter
- Samples in die or ROSA format

ADN2892 4 Gbps Limiting Amp with BW Select

- Bandwidth select function to support 1×, 2× Fibre Channel
- 3.2 Gbps BW
- 3.3 V, 140 mW
- RSSI function works with any standard ROSA
- 3 mm × 3 mm LFCSP
- LOS invert to support SFP and SFF

ADN2871 Single-Loop LDD

- Operation from 155 Mbps to 4.25 Gbps
- DFB, FP, or VCSEL operation
- Voltage setpoints simplify design
- Supports all SFF-8472 digital diagnostics requirements
- Pin-compatible with ADN2870 LDD

ADN2870 Dual-Loop LDD

- Operation from 155 Mbps to 4.25 Gbps
- Dual-loop eliminates need for temperature calibration and compensates for aging
- 3.3 V operation, 4 mm × 4 mm LFCSP package
- Supports all SFF-8472 digital diagnostics
- Pin-compatible with ADN2871

ADN2880 3.3 Gbps TIA with –24 dBm Sensitivity

- 250 nA input referred noise
- 3.5 kΩ transimpedance
- 75 mW power consumption

155 Mbps to 2.7 Gbps SFP reference design also available

ADN2891 3.3 Gbps Limiting Amp with 3 mV Sensitivity

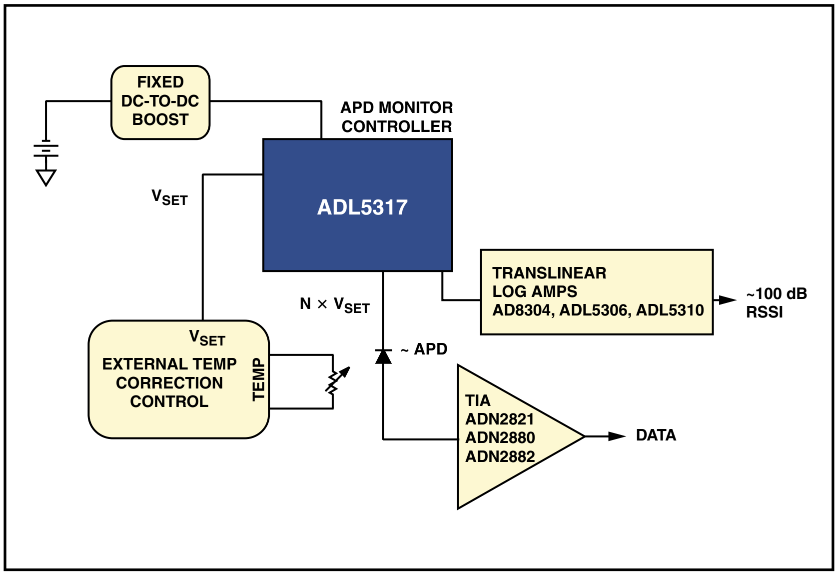
- RSSI function works with any standard ROSA
- Low power, 130 mW
- 3 mm × 3 mm LFCSP

ADL5317 APD Bias Controller

New Wide Dynamic Range APD Bias Controller and Current Monitor for Simpler, Low Noise Designs of APD Modules and Systems

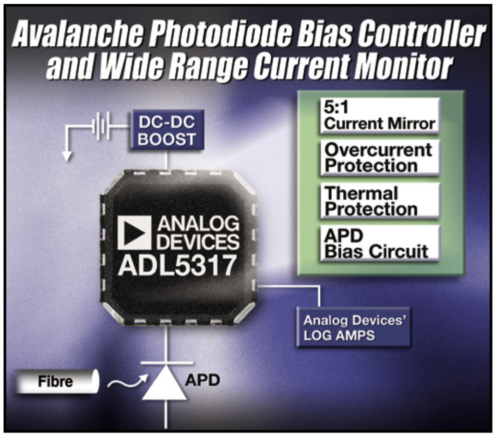
With the advent of higher speed optical networks, transceivers often employ avalanche photodiodes (APDs) as the photodetector to improve receiver sensitivity and increase link reach. Traditionally, biasing and control of APDs in optical circuits have been challenging. To use the APD for received signal indication, it is necessary to maintain a constant responsivity (A/W). Reducing the nonlinear variations of the APD over temperature is accomplished by accurately controlling its avalanche multiplication factor by changing the bias voltage.

The new ADL5317 avalanche photodiode bias controller and current mirror has been specifically designed for wide dynamic range applications simplifying APD bias circuits. The ADL5317 accurately sets APD bias voltage ranging from 6 V to 72 V, and simultaneously enables highly accurate monitoring of photodiode current over a 6-decade range. The linear bias control interface of the ADL5317 allows for optical designers to use a fixed high voltage switcher, reducing supply decoupling and low-pass filtering requirements necessary in traditional APD biasing designs due to switching noise created by PWM-based dc-to-dc converters. Incorporating features such as overcurrent protection and overtemperature shutdown, the device is built for exceptional performance over temperature and ease of design for all APD modules and systems.



Features

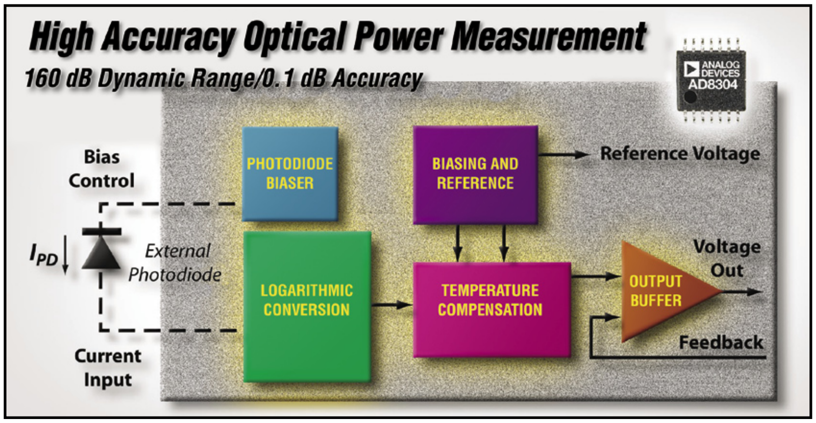
- Stable, high voltage bias range, 6 V to 72 V
- Control APD bias using 3 V-compatible V_{SET} interface
- Monitors photodiode current over 6-decade range
- Linearity 1% from 50 nA to 1 mA, 5% from 5 nA to 5 mA
- Overcurrent protection and over-temperature shutdown
- 16-lead, 3 mm × 3 mm chip scale package (LFCSP)



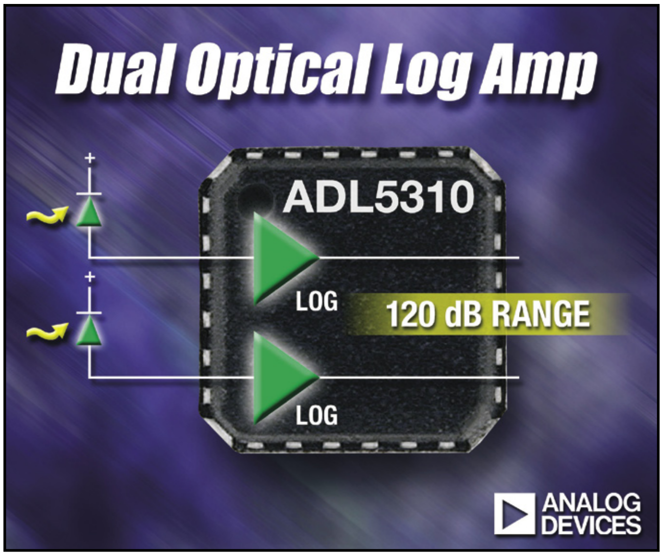
Optical Power Measurement Logarithmic Amplifiers

The industry's most complete range of logarithmic amplifiers for optical power measurements—whether it's easier design, higher dynamic range, board space savings, or lower design cost—Analog Devices has the right log amp for your optical measurement needs.

- AD8304: Our highest performance optimized log amp provides 0.1 dB of accuracy over 8 decades of measurement range. Available in 14-lead TSSOP.
- AD8305: In a smaller 3 mm × 3 mm chip scale package, the AD8305 provides 0.1 dB of accuracy over 100 dB of dynamic range.
- ADL5306: For cost-sensitive lower dynamic range needs in optical power measurement applications, the ADL5306 provides high accuracy over 60 dB of dynamic range.
- ADL5310: For cost and board space savings without compromising higher performance up to 120 dB of dynamic range, the dual log amp ADL5310 in a 4 mm × 4 mm chip scale package is the unbeatable choice.



AD8304



ADL5310

Features

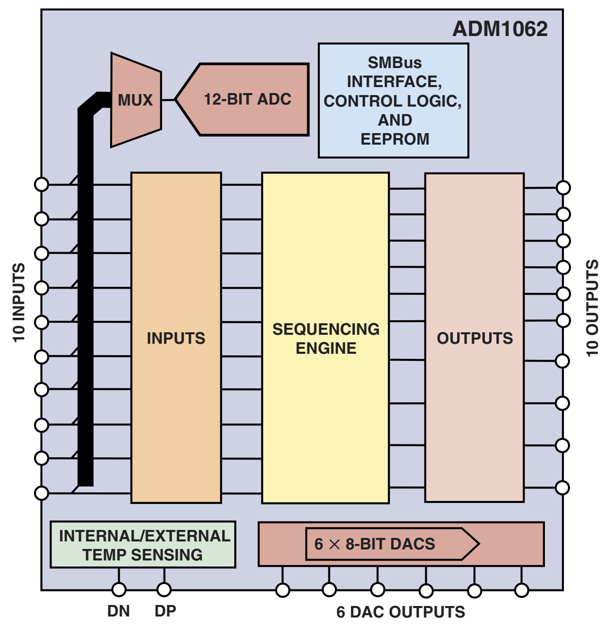
- Direct photodiode interface
- High accuracy over range/temperature
- Choice of dynamic range
- Linear-in-dB output
- Single power supply
- Small package

Applications

Analog Devices' family of logarithmic amplifier ICs employs an innovative translinear approach to achieve high dynamic range and accuracy. They can be used in a wide range of optical networking measurement and control applications, including optical amplifiers, optical switches, transmit laser modules, OADM, and SFF transceivers.

ADM106x Family: Multisupply Super Sequencers™ with Margining Control

ADI's Super Sequencer family consists of configurable supervisory and sequencing devices that offer a single chip solution for supply monitoring and sequencing in multisupply systems. The devices offer up to 10 programmable supply voltage monitor inputs, and ranges from 0.6 V to 14.4 V can be detected directly. Five of the inputs can also be configured as general-purpose logic inputs. An on-chip, 12-bit ADC allows readback of the supply voltages, offering an extra level of supply supervision that can be used in a closed-loop system with four or six on-chip DACs for supply voltage adjustment and margining. The ADM106x family has a versatile, programmable state machine-based sequencing engine. To store configuration parameters, 512 bytes of on-chip EEPROM are available.



Features

- Up to 10 supply fault detector inputs with programmable thresholds (±1% accuracy)
- Up to 5 general-purpose logic inputs
- 10 fully programmable output drivers
- Internal charge pump for high-side drive of N-channel FET on 6 outputs
- Flexible, programmable state machine-based sequencing engine
- Supply margining tools:
  - 12-bit ADC monitors, all supervised voltages
  - 6 V output DACs
  - Industry-standard SMBus interface
  - Internal and remote temperature sensing
- LFCSP and TQFP packages available

Applications

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

SUPER SEQUENCERS

Part Number	Supervising Accuracy	Sequencing	Monitor Inputs	Enable Outputs	Voltage Readback and Margining	Temp Sensing	Package	Price ($U.S.)*
ADM1060	±2.5%	Combinational Logic	7	9	–	–	28-Lead TSSOP	5.00
ADM1062	±1%	State Machine	10	10	12-Bit ADC + 6 DACs	±2°C	40-Lead LFCSP/ 48-Lead TQFP	7.50
ADM1063	±1%	State Machine	10	10	12-Bit ADC	±2°C (×2)	40-Lead LFCSP/ 48-Lead TQFP	6.98
ADM1064	±1%	State Machine	10	10	12-Bit ADC	–	40-Lead LFCSP/ 48-Lead TQFP	6.60
ADM1065	±1%	State Machine	10	10	–	–	40-Lead LFCSP/ 48-Lead TQFP	4.75
ADM1066	±1%	State Machine	10	10	12-Bit ADC + 6 DACs	–	40-Lead LFCSP/ 48-Lead TQFP	7.15
ADM1067	±1%	State Machine	10	10	6 DACs	–	40-Lead LFCSP/ 48-Lead TQFP	5.50
ADM1068	±1%	State Machine	8	8	–	–	32-Lead LFCSP/ 32-Lead TQFP	3.40
ADM1069	±1%	State Machine	8	8	12-Bit ADC + 4 DACs	–	32-Lead LFCSP/ 32-Lead TQFP	3.65

**In quantities of 10,000.*

Selection Table

Amplifiers

Part Number				Supply Voltage						Rail-to-Rail		Micro-packaging	A_{CL} Min	Bandwidth @ A_{CL} (MHz)	Slew Rate	Distortion SFDR @ Bandwidth R_L			Noise (nV/√Hz)	V_{OS} (mV Max)	I_B (mA Max)	$I_{S/AMP}$ (mA Typ)
Single	Dual	Triple	Quad	Disable	3 V	5 V	±5 V	±12 V	±15 V	In	Out					dBc	MHz	Ω				
AD8065	AD8066					•	•	•			•	•	1	145	180	–88	1	1k	7	1.5	10 pA	6.4
AD8067						•	•	•			•	•	8	60	500	–90	1	1k	7	1	10 pA	6.4

Fiber Optic Transimpedance Amplifiers

Part Number	Description	–3 dB Bandwidth (MHz)	Transimpedance (kΩ)	Supply Voltage (V)	Power Dissipation (mW)	Current Noise (pA/√Hz)	Overload Current (dBm)	Total Jitter (ps p-p)	Output Return Loss (dB)	Die Size (mm × mm)
AD8015	155 Mbps TIA	240	20	+5	125	3	350	—	—	1 × 1
ADN2880	3.3 Gbps TIA	2.3	5	+3.3	75	8	3.25	—	–20	0.7 × 1.2
ADN2882	4.25 Gbps TIA	3.2	4	+3.3	75	10	—	—	–20	0.7 × 1.2
ADN2821	10 Gbps TIA	9.5	10	+3.3	150	12	3.25	5	–12	0.7 × 1.2

Fiber Optic Limiting Amplifiers

Part Number	Description	Data Rate (Gbps)	Supply Voltage (V)	Input Sensitivity (mV p-p)	Power Dissipation (mW)	Output Levels (mV p-p diff)	LOS	Jitter (rms)	Squelch	BW Select	RSSI	Package
ADN2891	3.3 Gbps Limiting Amp	3.2	3.3	3	145	700	3 mV to 45 mV	2.4	Yes	No	Yes	3 mm × 3 mm LFCSP
ADN2892	4.25 Gbps Limiting Amp	4.25	3.3	3	160	700	3 mV to 45 mV	5	No	Yes	Yes	3mm × 3 mm LFCSP

Fiber Optic Laser Diode Drivers

Part Number	Description	Data Rate (Gbps)	Supply Voltage (V)	Laser Bias Current (mA)	Single-Ended/ Differential	Modulation Current (mA)	Rise/Fall Time (ps)	Dual Loop	MSA Compliance	Package
ADN2848	1.25 Gbps Dual-Loop LDD	1.25	3.3	100	Both	80	80	Yes	SFF	5 mm × 5 mm LFCSP
ADN2841	2.5 Gbps Dual-Loop LDD	2.7	5	100	Both	80	80	Yes	SFF	5 mm × 5 mm LFCSP
ADN2847	3.3 Gbps Dual-Loop LDD	3.3	3.3	100	Both	80	80	Yes	SFF	5 mm × 5 mm LFCSP
ADN2870	4.25 Gbps Dual-Loop LDD	3.3	3.3	100	Both	90	60	Yes	SFP-SFF-8472	4 mm × 4 mm LFCSP
ADN2871	4.25 Gbps Single-Loop LDD	3.3	3.3	100	Both	90	60	No	SFP-SFF-8472	4 mm × 4 mm LFCSP
ADN2525	10 Gbps Differential LDD	10.7	3.3	100	Differential	80	24	No	XFP, Xenpak, X2, MSA-300	3 mm × 3 mm LFCSP
ADN2530	10 Gbps VCSEL Driver	10.7	3.3	22	Differential	22	24	No	XFP, Xenpak, X2, MSA-300	3 mm × 3 mm LFCSP
ADN2830	CW Laser Driver	—	5	200	Single-Ended	—	—	—	—	5 mm × 5 mm LFCSP

Clock and Data Recovery ICs

Part Number	Description	Supply Voltage (V)	Data Rate (Gbps)	Power Dissipation (mW)	Input Sensitivity (mV p-p)	Jitter Tolerance (UI p-p)	Jitter Transfer	Jitter Generation (mUI rms)	Limiting Amp	Rate	Package
AD800	52 Mbps CDR	+5/–5.2	0.052	650	80	0.9 @ 65 kHz	52 kHz	7	No	Single	20-Lead SOIC
AD807	155 Mbps CDR	5	0.155	170	2	1.0 @ 65 kHz	92 kHz	5	Yes	Single	16-Lead SOIC
AD808	622 Mbps CDR	5	0.622	400	4	0.6 @ 250 kHz	333 kHz	7	Yes	Single	16-Lead SOIC
ADN2807	155 Mbps/622 Mbps CDR	3.3	0.155/0.622	540	4	1.0 @ 250 kHz	140 kHz @ OC12	1	Yes	Multi	7 mm × 7 mm LFCSP
ADN2811	2.5 Gbps/2.7 Gbps CDR	3.3	2.5/2.7	540	4	1.0 @ 1 MHz	590 kHz @ OC48	2	Yes	Dual	7 mm × 7 mm LFCSP
ADN2812	12.3 Gbps to 2.7 Gbps CDR	3.3	12.3 to 2.7	750	6	1.0 @ 1 MHz	490 kHz @ OC48	1	Yes	Continuous	5 mm × 5 mm LFCSP
ADN2813	12.3 Gbps to 1.25 Gbps CDR	3.3	12.3 to 1.25	425	6	1.0 @ 637 kHz	71 kHz @ OC12	1	Yes	Continuous	5 mm × 5 mm LFCSP
ADN2814	12.3 Mbps to 675 Mbps CDR	3.3	12.3 to 0.675	425	6	1.0 @ 250 kHz	71 kHz @ OC12	1	Yes	Continuous	5 mm × 5 mm LFCSP
ADN2815	12.3 Gbps to 1.25 Gbps CDR	3.3	12.3 to 1.25	375	50	1.0 @ 250 kHz	71 kHz @ OC12	1	No	Continuous	5 mm × 5 mm LFCSP
ADN2816	12.3 Mbps to 675 Mbps CDR	3.3	12.3 to 0.675	375	50	1.0 @ 250 kHz	71 kHz @ OC12	1	No	Continuous	5 mm × 5 mm LFCSP
ADN2819	155 Mbps to 2.7 Gbps CDR	3.3	2.7	540	4	1.0 @ 1 MHz	590 kHz @ OC48	2	Yes	Multi	7 mm × 7 mm LFCSP
ADN2928	9.9 Gbps to 11.3 Gbps TxRx Signal Conditioner	3.3/1.8	9.9 to 11.1	750	6	1.0 @ 1 MHz	2 MHz @ OC192	6	Yes	Continuous	6 mm × 6 mm BGA
ADN2927	9.9 Gbps to 11.3 Gbps Transmit Signal Conditioner	3.3/1.8	9.9 to 11.1	375	6	1.0 @ 1 MHz	2 MHz @ OC192	6	Yes	Continuous	4 mm × 4 mm LFCSP
ADN2926	9.9 Gbps to 11.3 Gbps Receive Signal Conditioner	3.3/1.8	9.9 to 11.1	375	6	1.0 @ 1 MHz	2 MHz @ OC192	6	Yes	Continuous	4 mm × 4 mm LFCSP

Analog-to-Digital Converters[1]

Part Number	Resolution (Bits)	Throughput Rate (kSPS)	Number of Analog Inputs	Power Supply Voltage (V_{NOM})	Power Dissipation (mW Max)	Reference (Int/Ext)	Description
AD7674	18	1,000	1	Single (5)	125	Int/Ext	18-Bit, 1 MSPS PulSAR® ADC
AD7621	16	Up to 3,000	1	Single (2.5)	100	Int	16-Bit, 1 LSB INL, 3 MSPS PulSAR ADC
AD7664/AD7665	16	570	1	Single (5)	115/107	Ext	16-Bit, 570 kSPS, PulSAR ADC ADC
AD7671	16	1,000	1	Single (5)	125	Ext	16-Bit, 1 MSPS, Bipolar PulSAR ADC
AD7676	16	500	1	Single (5)	74	Ext	16-Bit, 500 kSPS, Differential PulSAR ADC
AD7865	14	350	4	Single (5)	130	Ext	14-Bit, 4-Channel Simultaneous Sampling Parallel ADC
AD7484	14	3,000	1	Single (2.3 to 5.25)	90	Int	14-Bit, 3 MSPS Parallel ADC
AD7856	14	285	8	Single (5)	12.5	Int	14-Bit, 8-Channel, 285 kSPS Serial ADC
AD7490	12	1,000	16	Single (2.7 to 5.25)	6	Ext	12-Bit, 16-Channel, 1 MSPS Serial ADC with Sequencer
AD7927	12	200	8	Single (2.7 to 5.25)	3.6	Ext	12-Bit, 8-Channel, Serial ADC with Sequencer

Digital-to-Analog Converters

Part Number	Resolution (Bits)	Number of DACs	Input	Output	Power Supply	Package	Description
AD5379	14	40	Serial/Parallel	V_{OUT} (Bipolar)	±12 V and 3 V or 5 V	CSPBGA-108	14-Bit, 40-Channel, Bipolar V_{OUT} DAC
AD5380	14	40	SPI®/I²C®/Parallel	V_{OUT}	2.7 V to 5.5 V	LQFP-100	14-Bit, 40-Channel, Single-Supply DAC
AD5532	14	32	Serial 3-Wire (SPI)	V_{OUT} (Bipolar)	+5 V, ±15 V	CSPBGA-74	14-Bit, 32-Channel, Serial DAC
AD5532HS	14	32	Serial 3-Wire (SPI)	V_{OUT} (Bipolar)	+5 V, ±15 V	CSPBGA-74	14-Bit, 32-Channel, Fast Serial DAC
AD5535	14	32	SPI	V_{OUT}	200 V, 5 V	CSPBGA-108	14-Bit, 32-Channel, 200 V DAC
AD5382	14	32	SPI/I²C/Parallel	V_{OUT}	2.7 V to 5.5 V	LQFP-100	14-Bit, 32-Channel, Single-Supply DAC
AD5390	14	16	SPI/I²C	V_{OUT}	2.7 V to 5.5 V	LFCSP-64, LQFP-52	14-Bit, 16-Channel, Single-Supply DAC
AD5392	14	8	SPI/I²C	V_{OUT}	2.7 V to 5.5 V	LFCSP-64, LQFP-52	14-Bit, 8-Channel, Single-Supply DAC
AD7841	14	8	Parallel	V_{OUT} (Bipolar)	±15 V	PQFP-44	14-Bit, 8-Channel, Parallel DAC
AD5516	12	16	Serial 3-Wire (SPI)	V_{OUT} (Bipolar)	±5 V, ±15 V	CSPBGA-74	12-Bit, 16-Channel, Serial DAC
AD5328	12	8	Serial 3-Wire (SPI)	V_{OUT}	2.7 V to 5.5 V	TSSOP-16	12-Bit, 8-Channel, Serial Single-Supply DAC

MicroConverters®

Part Number	ADC	DAC	MCU	Flash/EE Code	Package	Special Features
ADuC7020/ADuC7021/ADuC7022	5-/8-/10-Channel, 12-Bit	Multichannel, 12-Bit	16-Bit/32-Bit RISC	62 kB, 32 kB	CSP-40	ARM7TDMI Core, Small Footprint
ADuC812	8-Channel, 12-Bit	Dual, 12-Bit	12-Clock 8052	8 kB	PQFP-52, CSP-56	5 µs ADC
ADuC814	6-Channel, 12-Bit	Dual, 12-Bit	12-Clock 8052	8 kB	TSSOP-28	Small, Low Cost
ADuC831	8-Channel, 12-Bit	Dual, 12-Bit + Dual PWM	12-Clock 8052	62 kB	PQFP-52, CSP-56	Big Memory Upgrade to ADuC812
ADuC832	8-Channel, 12-Bit	Dual, 12-Bit + Dual PWM	12-Clock 8052	62 kB	PQFP-52, CSP-56	Same as ADuC831, but with PLL Clock
ADuC841	8-Channel, 12-Bit	Dual, 12-Bit + Dual PWM	12-Clock 8052	62 kB	PQFP-52, CSP-56	Fast Core Upgrade to ADuC831 (no PLL)
ADuC842	8-Channel, 12-Bit	Dual, 12-Bit + Dual PWM	12-Clock 8052	62 kB	PQFP-52, CSP-56	Fast Core Upgrade to ADuC832 (with PLL)

Control and Monitoring ICs

Part Number	Performance	Package	Description
AD8304	160 dB Range (100 nA to 10 mA)	TSSOP-14	Logarithmic Amplifier with Photodiode Interface
AD8305	100 dB Range (10 nA to 1 mA)	LFCSP-16	Logarithmic Amplifier with Photodiode Interface
ADL5306	60 dB Range (100 nA to 100 mA)	LFCSP-16	Logarithmic Amplifier with Photodiode Interface
ADL5310	120 dB Range (3 nA to 3 mA)	LFCSP-24	Dual Logarithmic Amplifier with Photodiode Interface
ADL5317	120 dB Range (5 nA to 5 mA) Current Monitoring, APD Bias Range from 6 V to 72 V	LFCSP-16	Avalanche Photodiode Bias Controller and Wide-Range Current Monitor
ADN8810	Current Output (0 to 250 mA)	LFCSP-24	Programmable Precision Current Source for Tunable Lasers
ADN8830	Low Noise: < 0.5% TEC Current Ripple	LFCSP-32	Thermoelectric Cooler Controller
ADN8831	Low Noise: <0.05% TEC Current Ripple	LFCSP-32	High Precision Thermoelectric Cooler Controller

Digital Crosspoint Switches

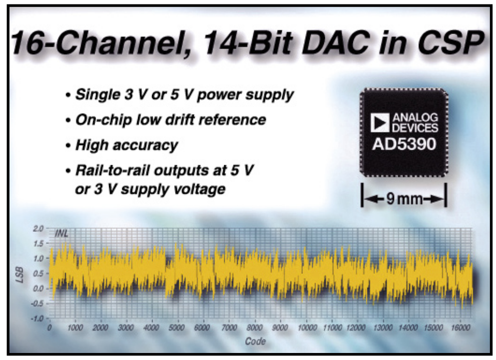
Part Number	Performance	Package	Function
AD8150	1.5 Gbps	LQFP-184	33 × 17 Digital Crosspoint Switch
AD8151	3.2 Gbps	LQFP-184	33 × 17 Digital Crosspoint Switch
AD8152	3.2 Gbps	BGA-256	34 × 34 Digital Crosspoint Switch
ADXS34	3.2 Gbps	EBGA-304	34 × 34 Synchronous Crosspoint Switch
AD8159	3.2 Gbps	TQFP-100	Quad 2:1 Mux/Demux

[1]Partial listing.

Single-Supply, 16-Channel and 8-Channel DACs Pack Performance and Functionality into a 9 mm × 9 mm CSP

High channel count DACs are ideally suited for power amplifier control, instrumentation, control systems, and level setting, or for any application where board space is at a premium. Only one supplier provides the channel density, high resolution, high accuracy, and wide range of features demanded by these challenging designs.

Analog Devices' new family of high density DACs provides the channel density, high resolution, high accuracy, and wide range of features demanded by these challenging designs. The AD5390 features the industry's first 16-channel, 14-bit resolution voltage-output DAC operating from either a single 5 V or 3 V power supply. A 12-bit version (AD5391) and an 8-channel, 14-bit version (AD5392) are also available. All devices are offered in a 64-lead LFCSP and a 52-lead LQFP.



These devices contain on-chip, low drift references (2.5 V and 1.25 V), eliminating the need for an external reference IC, and reducing cost and board space. The parts also include user-programmable offset and gain for digital range adjustment and system calibration. They offer high accuracy and increased functionality, including a boost mode that allows the parts to achieve faster settling times, and an LDAC (load DAC) function that allows simultaneous update of all DAC outputs.

ADI's high density DACs offer rail-to-rail outputs at a 5 V or 3 V supply voltage. In addition, they offer the choice of SPI and I²C serial interfaces, and are pin-for-pin compatible, allowing a designer the option of generating different grades of end product as appropriate. Visit our website for more information on samples and evaluation boards at *www.analog.com/denseDACs*.

Applications

- Optical line cards
- Variable optical attenuators
- Instrumentation and industrial control
- Power amplifier control
- Level setting
- Control systems
- Medical equipment

Part Number	Channels	Resolution (Bits)	INL (LSB)	Power Supply (V)	Package	Price ($U.S.)
AD5390-5/AD5390-3	16	14	±4	5/3	64-Lead LFCSP, 52-Lead LQFP	23.90
AD5391-5/AD5391-3	16	12	±1	5/3	64-Lead LFCSP, 52-Lead LQFP	19.90
AD5392-5/AD5392-3	8	14	±4	5/3	64-Lead LFCSP, 52-Lead LQFP	14.90

New Single-Supply, 40-Channel DAC Packs Performance and Functionality into 10 mm × 10 mm CSPBGA

High channel count DACs are ideally suited for instrumentation, level setting, laser control, or any application where board space is at a premium.

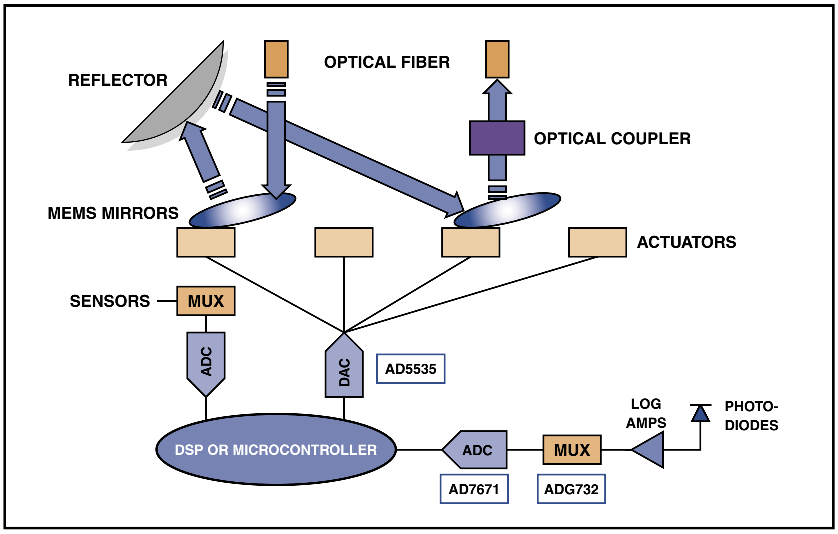
The AD5384 is an extension of the AD5380 and AD5390 family of high density DACs. The new AD5384 features the industry's first 40-channel, 14-bit resolution voltage-output DAC with a 10 mm × 10 mm footprint. This device operates from either a single 5 V or 3 V power supply and provides rail-to-rail outputs. It offers a choice of SPI and I²C serial interfaces.

The AD5384 contains on-chip, low drift references (2.5 V and 1.25 V) that eliminate the need for an external reference IC, reducing cost and board space. The part also includes user-programmable offset and gain per channel for digital range adjustment and system calibration. It offers high accuracy and increased functionality, including a boost mode that allows the parts to achieve faster settling times, a monitor mode that multiplexes the analog outputs to a single pin, and an LDAC function that allows simultaneous update of all DAC outputs. For more information, visit *www.analog.com/denseDACs*.

Part Number	Channels	Bits	INL (LSB)	Power Supply (V)	Package	Price ($U.S.)
AD5384-5/ AD5384-3	40	14	±4	5/3	CSPBGA-100	49.50
AD5380-5/ AD5380-3	40	14	±4	5/3	LQFP-100	49.50
AD5381-5/ AD5381-3	40	12	±1	5/3	LQFP-100	39.50

High Voltage, 32-Channel DAC in 15 mm × 15 mm Footprint for MEMS Mirror Control

The AD5535 is a 32-channel, 14-bit DAC with on-chip high voltage output amplifiers. This device is ideally suited for the control of MEMS devices in optical crosspoint switches or variable optical attenuators (VOAs). The AD5535 is guaranteed monotonic to 14 bits. Its output voltage range is programmable via the REF_{IN} pin, e.g., the output range is 0 V to 50 V with REF_{IN} = 1 V and is 0 V to 200 V with REF_{IN} = 4 V. Each output amplifier can source 700 µA, ideal for the deflection and control of optical MEMS mirrors. Each amplifier has a gain of 50 and is driven from a 14-bit DAC whose output range varies from 0 to V_{REF} depending on the code loaded to the relevant DAC register. The selected DAC register is written to via the 3-wire SPI interface, which operates at clock rates up to 30 MHz.



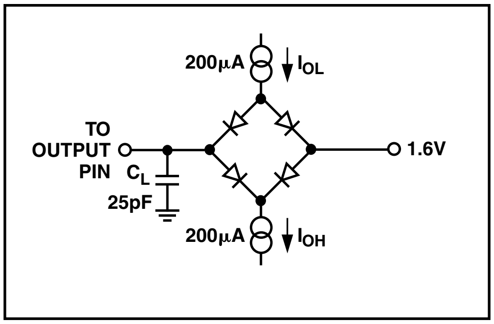
The AD5535 operates with AV_{CC} = 5 V, DV_{CC} = 3 V to 5 V, V– = –5 V, V+ = +5 V, and V_{PP} = 210 V. It is packaged in a 124-CSPBGA package with a footprint of 15 mm × 15 mm. For more information, visit *www.analog.com/AD5535*.

Need More Channels? We've Added a 16-Channel Mux with Sequencer to the Lowest Power, 1 MSPS, 12-Bit ADC.

In the optical communications sector there is a major demand for increased channel count on ADCs. With this increased channel count is a need to be able to select between channels and program various channel sequences for the ADC to convert.

The AD7490 is a 12-bit, 1 MSPS, low power successive approximation ADC. The AD7490 features 16 single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially. These channels can be selected by programming the relevant bits in the shadow register.

The AD7490 operates from a single 2.7 V to 5.25 V supply, and contains the V_{DRIVE} function, allowing the serial interface to connect directly to either 3 V or 5 V processor systems independent of V_{DD}. The analog input for the part can be selected to be 0 to REF_{IN} or 0 to 2× REF_{IN} with either straight binary or twos complement output coding. The AD7490 features a number of shutdown modes to maximize further power efficiency at lower throughput rates and is available now for $5.95 in 1k quantities.



Load Circuit for Digital Output Timing Specifications

Part Number	Resolution (Bits)	Throughput (kSPS)	Power (mW Max)	Channels
AD7490	12	1,000	12.5	16
AD7928	12	1,000	13.5	8
AD7927	12	200	7.5	8
AD7918	10	1,000	13.5	8
AD7908	8	1,000	13.5	8
AD7924	12	1,000	13.5	4
AD7923	12	200	7.5	4
AD7914	10	1,000	13.5	4
AD7904	8	1,000	13.5	4

Features

- Fast throughput rate: 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- 5.4 mW max at 1 MSPS with 3 supplies
- 12.5 mW max at 1 MSPS with 5 V supplies
- 16 (single-ended) inputs with channel sequencer
- Available in 28-TSSOP and 32-LFCSP packages

Applications

- Optical networking
- Instrumentation
- Data acquisition

ADSX34 Synchronous Crosspoint Switch

Difficult signal integrity, density, and low power design challenges are inherent in packet and cell-based switching and routing systems that drive enterprise/SAN and access and metro networks. Network equipment suppliers must address these challenges and develop unified, low cost, flexible multiprotocol switching solutions that can scale from enterprise to edge aggregation and core applications.

The ADSX34 is the industry's lowest power, synchronous crosspoint switch. The new chip is designed to solve difficult signal integrity, density, and low power design challenges, while enabling designers to develop equipment on time, on budget, and with system flexibility. At 5 W, the ADSX34 consumes one-third the power of comparable products on the market. The device, part of ADI's X*stream*™ family of low power crosspoint switches, integrates 34 SERDES channels, equalization, and other features, making it a complete solution for high speed networks. The device's low power consumption reduces the need for expensive, space-consuming heat sinks and other thermal management components.

Feature-Rich Crosspoint Switch

The ADSX34 Is a Feature-Rich, Complete Crosspoint Solution that Offers:

- 34 highly integrated channels, each operating at up to 3.2 Gbps
- Per channel programmable receive equalization and transmit pre-emphasis that allows equalization over 30 inches of FR4 material, including two standard high density differential connectors
- Support for time slots of 24 to 4,000 characters
- Per channel time slot synchronization FIFOs absorb up to 128 bytes of variation in packet arrival times, simplifying system timing

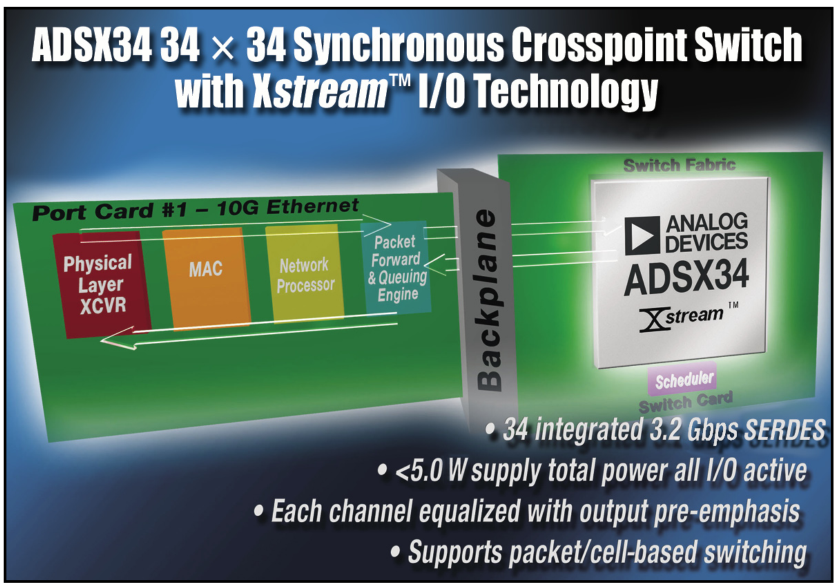
Flexibility Is Key for Networking Applications

The versatility of the ADSX34 makes it ideal for multiservice environments. The ADSX34 can switch any form of packet or cell-based traffic, including ATM (asynchronous transfer mode), Ethernet, Fibre Channel, serial rapid I/O, or IP (Internet protocol), eliminating the need to design multiple switches for different protocols.

Applications

- Packet and cell-based switching and routing systems that drive enterprise/SAN and access and metro networks

X*stream*™



AD8159 Four-Lane 2:1 Multiplexer/Demultiplexer

System designers of today's modular communications face an increasingly difficult challenge of supplying high reliability systems and reducing downtime. One of the most effective methods to achieve this is by designing built-in redundancy.

The AD8159 is the most cost-effective method to offer redundant switching within a modular communications system. The AD8159 is tailored to support redundancy on both the backplane and the line interface. The device has unicast and bicast capability, so it can be configured to support either 1+1 or 1:1 redundancy.

The AD8159 is a member of Analog Devices' X*stream* line of digital crosspoints. It is an asynchronous, protocol agnostic, four-lane 2:1 multiplexer/demultiplexer with a total of 12 differential LVPECL-/CML-compatible inputs and 12 differential CML outputs. The integrated receive equalization and transmit pre-emphasis allow for directly driving legacy and next generation backplanes. The operation of this product is optimized for NRZ signaling with data rates up to 3.2 Gbps per lane.

The AD8159 is equipped with Analog Devices' proprietary crossover transceiver, which allows for swapping transmit and receive pairs to greatly ease layout and compatibility issues.

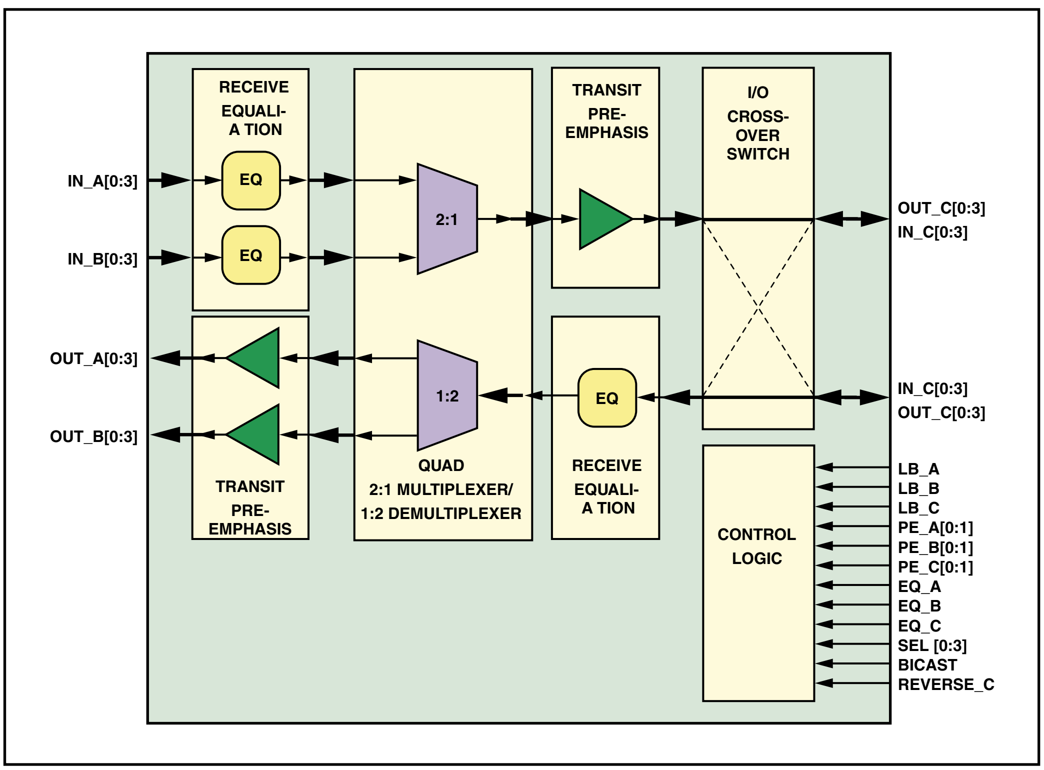
Xstream™

Features

- 4-lane 2:1 mux/1:2 demux
- Quad- or single-lane switching
- Port-level loopback
- Programmable input equalization
- Programmable output pre-emphasis
- Asynchronous operation
- Simple control interface
- 0 Gbps to 3.2 Gbps data rate
- 1 W total power dissipation
- 3.3 V power supply
- LVPECL-/CML-compatible inputs
- 100-lead TQFP package

Applications

- Switch fabric redundancy
- Backplane equalization
- Loopback diagnostics
- Fan-in/out
- Ethernet
- Fibre Channel
- Infiniband
- SONET/SDH



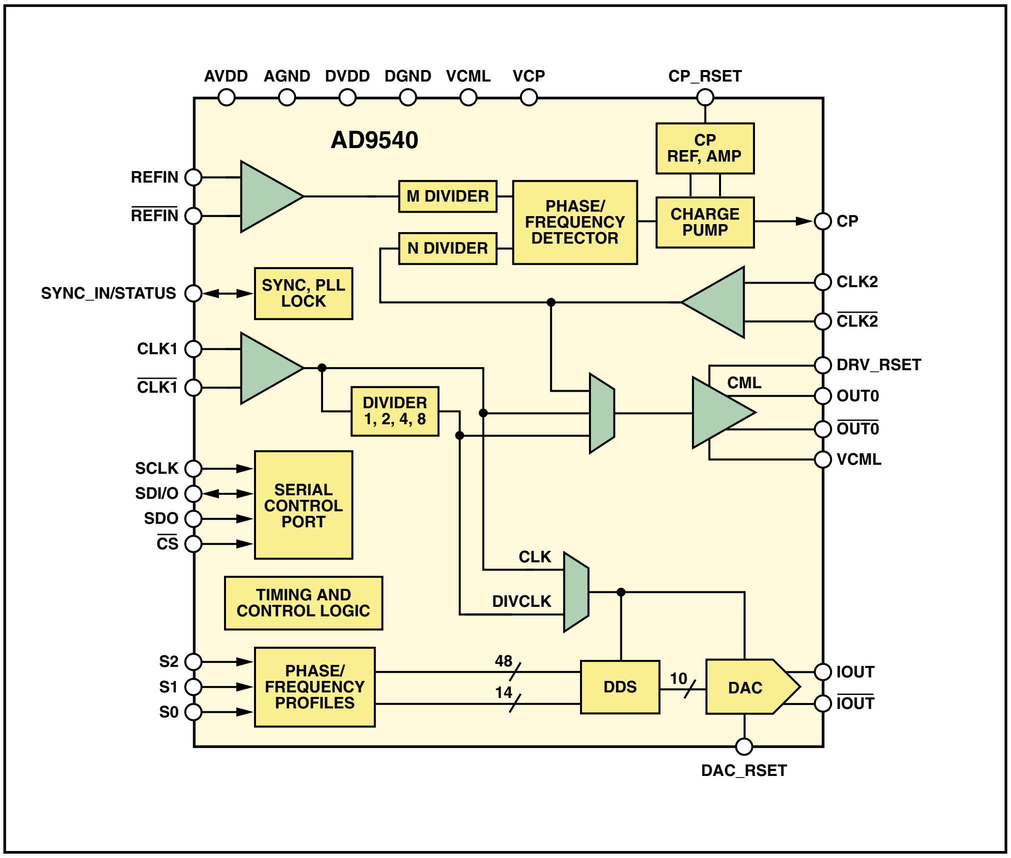
Generating Multiple Clock Outputs from the AD9540

In today's digital and mixed-signal electronic systems, clocking is an important consideration for overall system performance. The ability to generate clocks at specific rates with low jitter is vital to the proper functioning of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). This is because uncertainty in the time domain, characterized as jitter, translates to uncertainty in amplitude, reducing the achievable noise floor and corresponding figures of merit, such as signal-to-noise ratio (SNR) and bit error rate (BER). Other challenges faced in generating clocks include frequency accuracy, frequency resolution, and the ability to introduce timing skew or phase delay between different channels.

To meet these challenges, Analog Devices offers a family of clock generation and clock distribution products. One of the first offerings, the AD9540, is a low jitter clock generation integrated circuit (IC). The AD9540 features a low jitter clock output from its current mode logic (CML) driver, capable of achieving rates of up to 655 MHz, suitable for clocking ADCs and DACs. Frequently, in a mixed-signal system, additional clocks are needed to clock digital hardware.

While jitter is not as much of a concern in strictly digital systems, the ability to provide precise frequency resolution and to introduce controlled delays on the rising edges of the clock waveform are important. What follows will demonstrate how to achieve a low jitter, high speed clock and a lower rate with programmable skew, all derived from a single AD9540 IC.

Examine the block diagram shown below. An overview of the included circuitry shows that many of the necessary component blocks are present in the AD9540 for generating both clocks needed. In generating low jitter clocks, it is almost always preferable to employ a phase-locked loop (PLL) circuit of some sort. Beyond providing frequency gain, PLL circuits offer great noise reduction capability since the loop filter acts as a tracking bandpass filter. In most clocking applications a single frequency is required, therefore, parameters such as acquisition time and tuning range are not of importance. Performance in these areas can be sacrificed to increase the noise performance of the loop. Specifically, a very narrow range VCO can be selected with a center frequency close to the desired

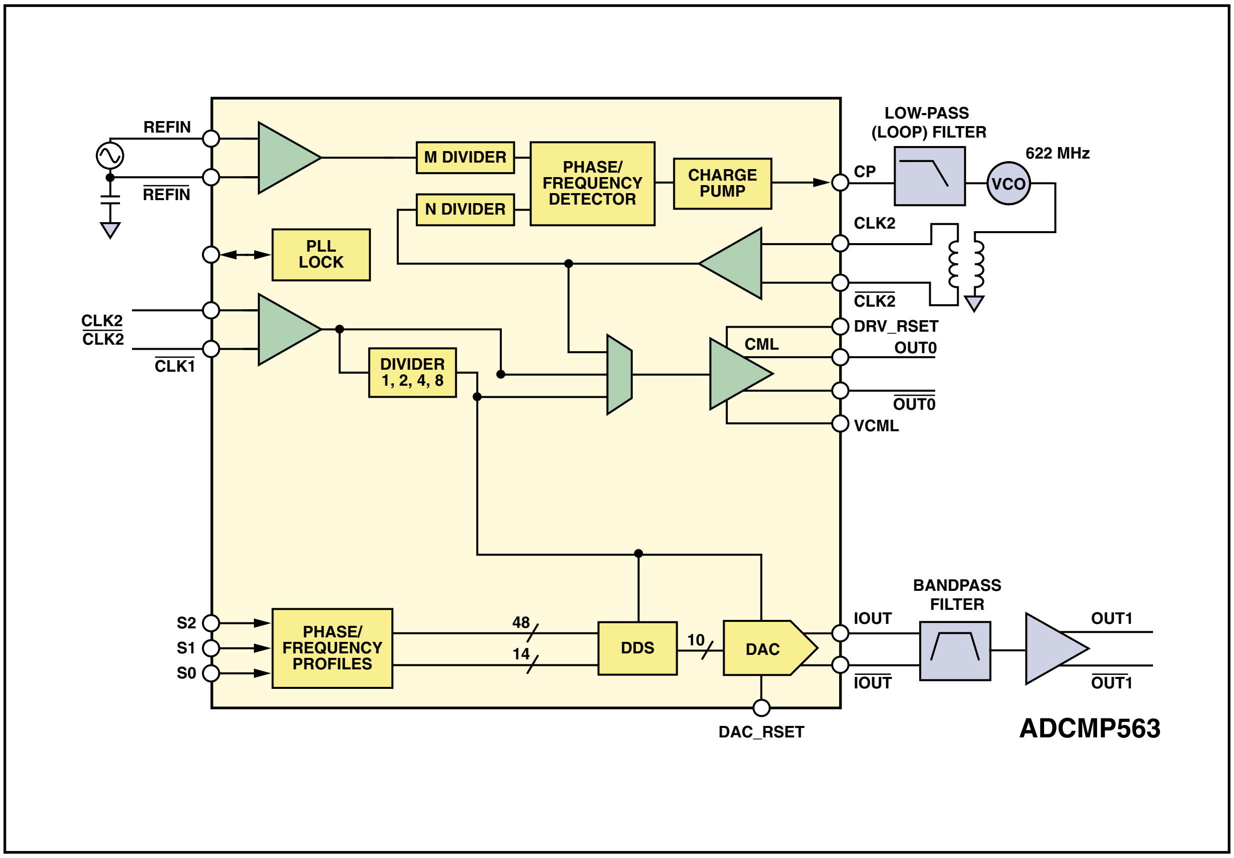


Functional Block Diagram

clock rate. As the tuning range is reduced, the gain coefficient for the VCO is reduced, and the phase noise of the VCO itself is thereby reduced. Also, the loop filter bandwidth is a concern for designers in that there is a trade-off associated with this parameter. Note that the wider the loop bandwidth, the faster the acquisition and lock time of a loop but the more noise from the reference and phase frequency detector itself gets fed through the loop. In the case of a clocking application, this trade-off can be made to achieve narrow loop bandwidths, sacrificing settling time in favor of noise suppression through the loop.

The digital clock, which requires precise frequency and adjustable phase, can be generated from the direct digital synthesizer (DDS) portion of the device. The DDS on the AD9540 offers 48-bit frequency tuning resolution (1.42 MHz, given the maximum clock rate of 400 MHz) and 10-bit phase adjustment (0.351 deg). The output of a DDS is a reconstructed sine wave, so two additional external circuits are required. First, a bandpass filter at the desired clock rate needs to be applied to the reconstructed sine wave. This removes all sampling artifacts from the output spectrum as well as broadband noise that has infected the DAC output signal. Second, to achieve the required slew rates for most clock circuits, an external comparator needs to be inserted into the clock signal path. One excellent choice, used for this example, is the ADCMP563.

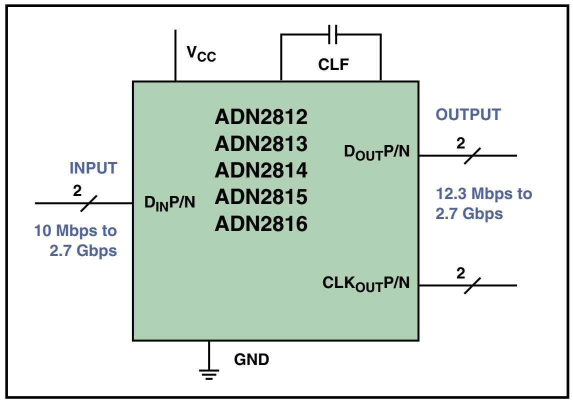
A simplified block diagram for the resultant circuit is shown below. The following are notes to the diagram that may not be readily apparent from the drawing. First, inputs Clock1/$\overline{\text{Clock1}}$ are shorted to Clock2/$\overline{\text{Clock2}}$. The device is programmed so that the CML driver gets its input from the undivided input from Clock 1, but the DDS is clocked by the divided output (622 MHz divided by 2 = 311 MHz). The two output clocks are shown at OUT0 (the low jitter 622 MHz clock) and OUT1 (the phase programmable auxiliary clock). Edge skew (or time delay) in the auxiliary clock is accomplished by programming a phase offset into the DDS, which will change the relative point in time for the complementary input crossing at the comparator.

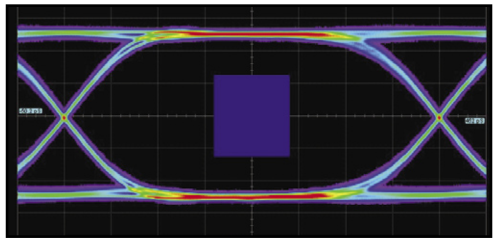


Solution Configuration

Continuous Tuning Family of Pin-Compatible CDRs

The ADI family of pin-compatible continuous tuning CDRs eases design complexity by providing industry-leading jitter generation, tolerance, and transfer combined with the features, flexibility, and price points for all fixed rate, multirate, and continuous tuning applications. No reference clock or external control is required for devices to lock to any NRZ signal within frequency range.



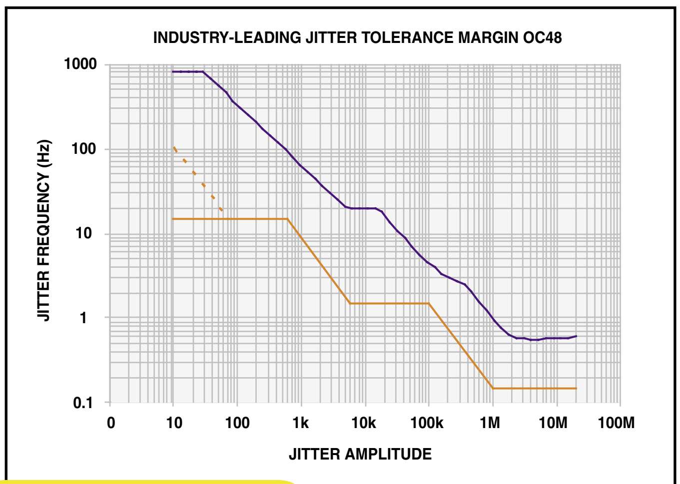


ADN2812

ADN2812 CDR with Limiting Amp

- Automatically locks to any data rate between 12.3 Mbps and 2.7 Gbps
- 6 mV input sensitivity
- Lowest jitter generation:
  - 0.001 UI rms jitter @ OC48
- Highest jitter tolerance:
  - 1.0 UI p-p @ 1 MHz OC48
- Lowest jitter transfer:
  - 490 kHz OC48
- Adjustable slice level
- Programmable LOS indicator
- LOL indicator
- 750 mW power dissipation
- No REF clock required
- Data rate readback function

All the performance and features of the ADN2812, half the power. Sampling now.



With ADI CDRs you don't have to settle. You get the industry's best J_{GEN}, J_{TRAN}, and J_{TOL}.

ADN2813 CDR with Limiting Amp

- Range: 12.3 Mbps to 1.25 Gbps
- 430 mW power dissipation

ADN2814 CDR with Limiting Amp

- Range: 12.3 Mbps to 675 Mbps
- 430 mW power dissipation

ADN2815 CDR

- Range: 12.3 Mbps to 1.25 Gbps
- 380 mW power dissipation

ADN2816 CDR

- Range: 12.3 Mbps to 675 Mbps
- 380 mW power dissipation

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